10 D74

H CRAIG
6/71 1st

758

WAVETEK

9045 BALBOA AVENUE, SAN DIEGO, CALIFORNIA

Serial No. _____

INSTRUCTION MANUAL

MODEL 755
PROGRAMMABLE
PHASE METER

WAVETEK
Box 651, San Diego, Calif., 714-279-2200
Box 1987, Indianapolis, Ind., 317-783-3221

6/71

WARRANTY

All Wavetek instruments are warranteed against defects in material and workmanship for a period of one year after date of manufacture. Wavetek agrees to repair or replace any assembly or component (except batteries) found to be defective, under normal use, during this period. Wavetek's sole opinion proves to be defective within the scope of the warranty when returned to the factory or to an authorized service center. Transportation to the factory or service center is to be prepaid by purchaser. Shipment should not be made without prior authorization by Wavetek.

This warranty does not apply to any products repaired or altered by persons not authorized by Wavetek, or not in accordance with instructions furnished by Wavetek. If the instrument is defective as a result of misuse, improper repair, or abnormal conditions or operations, repairs will be billed at cost.

Wavetek assumes no responsibility for its product being used in a hazardous or dangerous manner either alone or in conjunction with other equipment. High voltage used in some instruments may be dangerous if misused. Special disclaimers apply to these instruments. Wavetek assumes no liability for secondary charges or consequential damages and, in any event, Wavetek's liability for breach of warranty under any contract or otherwise, shall not exceed the purchase price of the specific instrument shipped and against which a claim is made.

Any recommendations made by Wavetek for use of its products are based upon tests believed to be reliable, but Wavetek makes no warranty of the results to be obtained. This warranty is in lieu of all other warranties, expressed or implied, and no representative or person is authorized to represent or assume for Wavetek any liability in connection with the sale of our products other than set forth herein.

CONTENTS

SECTION 1 – INTRODUCTION

1.1 PURPOSE OF THE EQUIPMENT 1-1
1.2 SPECIFICATIONS PHASE MEASUREMENT 1-1
1.3 SPECIFICATIONS GENERAL 1-3

SECTION 2 – INSTALLATION AND OPERATION

2.1 MECHANICAL INSTALLATION 2-1
2.2 ELECTRICAL INSTALLATION 2-1
2.3 OPERATING CONTROLS 2-3
2.4 PRELIMINARY CHECKS 2-4
2.5 OPERATION PROCEDURE 2-4

SECTION 3 – CIRCUIT DESCRIPTION

3.1 SIMPLIFIED BLOCK DIAGRAM 3-1
3.2 FUNCTIONAL BLOCK DIAGRAM ANALYSIS 3-2
3.3 SUPPLEMENTAL CIRCUITS 3-10

SECTION 4 – MAINTENANCE

4.1 ACCESS INSTRUCTIONS 4-1
4.2 CALIBRATION INSTRUCTIONS 4-1
4.3 CORRECTIVE MAINTENANCE 4-7

SECTION 5 – DIAGRAMS, ADDENDUMS AND PARTS LIST

5.1 DIAGRAMS 5-1
5.2 ADDENDUMS 5-1
5.3 PARTS LIST 5-1

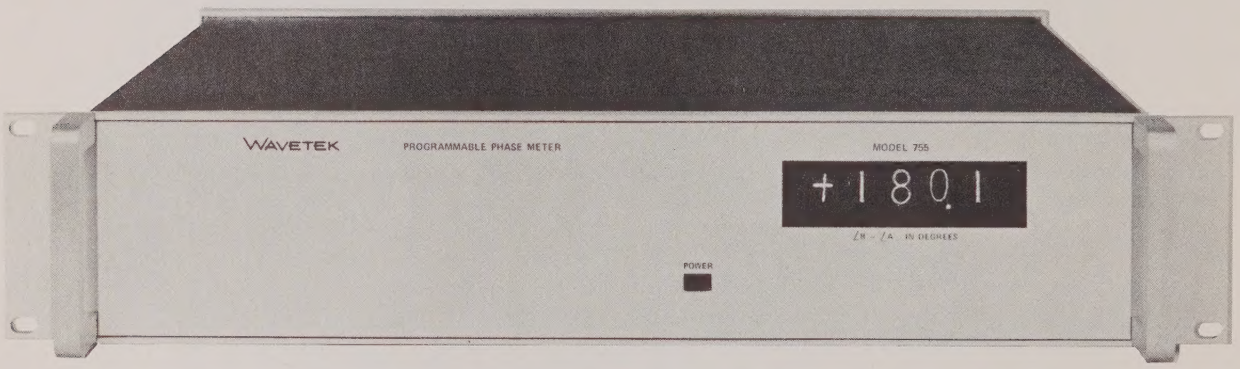


Figure i Model 755 Programmable Phase Meter

SCOPE OF THIS MANUAL

This manual provides descriptive material and instructions for the installation, operation, maintenance, and repair of this instrument. Wavetek's product improvement program ensures that the latest electronic developments are incorporated in all Wavetek instruments by the addition of circuit and component changes as rapidly as development and testing permit. Due to the time required to document and print instruction manuals, it is not always possible to incorporate the more recent changes in the released manual. In this case, data will be found on engineering change sheets at the rear of the manual. If no change sheets are included, the manual is correct as printed.

SECTION 1
INTRODUCTION

1.1 PURPOSE OF THE EQUIPMENT

The WAVETEK Model 755 PROGRAMMABLE PHASE METER is an automatic programmable phase meter especially designed for use in systems applications. The features of the Model 755 include the following:

Automatic Ranging (measurement)/Programmable Range

BCD Output(s)

External Read Command – which allows the system to update its digital readout only on command from an external source.

Programmable Calibrate Command

Programmable Amplitude Range

1.1.1 Measurement Mode

The Model 755 Programmable Phase Meter has been designed to accurately measure the phase angle between any two ac signals (with an amplitude dynamic range up to 1000 to 1) within the 40 Hz to 2 MHz range. A precision wideband instrument, the Model 755 uses a unique circuit design which permits accurate phase angle measurement with input signals having high even harmonic distortion. A four-digit readout is used to display, in degrees and tenths of degrees, the angle being measured.

Two ranges, 0°/360° and −180°/+180°, assure continuous phase data without discontinuity at 0 and 180 degrees. The auto ranging circuit incorporated in the Model 755 automatically changes the range to permit the best possible operation to alleviate the phase discontinuity problem. High impedance differential inputs are used; and a dc OUTPUT −10 mV/DEG is provided for use in recording phase angle measurements, or as a control signal for phase lock loops or servo systems. The BCD output is available on the rear of the instrument. Also the phase max-min calibrate programming is available which allows the user to program the maximum and minimum of the range selected to be read out on the digital display.

The automatic operation of this instrument eliminates the need for amplitude matching, frequency tuning, and output filtering, resulting in true hand-off phase measurements.

1.2 SPECIFICATIONS PHASE MEASUREMENT

1.2.1 Input Signals

Frequency Range . . . . . 40 Hz to 2 MHz

Absolute Calibration Accuracy
200 Hz to 20 kHz square wave, 100 mV to 5 V p-p. ±0.1°

Frequency Effect on Accuracy (100% of Range Sine Wave Inputs)
200 Hz to 20 kHz . . . . Calibration Accuracy ±0.2°
Zero Offset, 40 Hz to 10 kHz . . . . Less than 0.1°
Zero Offset, 10 kHz to 100 kHz . . Less than 0.1°/10 kHz
Relative Accuracy, 100 kHz to 2 MHz . . Better than 2°
Readout scatter is approximately 0.4° at 100 Hz, 0.6° at 50 Hz and 2° at 40 Hz.

OVERVOLTAGE LIMITS

Amplitude Ranges	AC Limit	Maximum Peak (AC + DC Limit)
.001-2 VOLTS RMS	50 V RMS	100 VOLTS
.300-300 VOLTS RMS	330 V RMS	500 VOLTS

Amplitude Effect on Accuracy (Equal Level Inputs)
Less than 1.5° for 60 dB change on both (A and B) inputs.

NOTE

1. *Minimum sensitivity above 50 kHz is 1% of full scale selected.*
2. *For frequencies above 20 kHz, both channel A and channel B should be programmed to the same range to eliminate attenuator phase delay.*

Phase Angle Resolution . . . . . 0.1°
Phase Angle Drift . . . . . Less than 0.3°/100 hours

Input Impedance
Single-Ended Inputs. . . . 1 MΩ, shunted by 30 pF
Differential Inputs . . . . 2 MΩ, shunted by 20 pF

Common Mode Rejection
40 Hz to 100 kHz . . . . . Greater than 50 dB
100 kHz to 2 MHz . . . . . Greater than 40 dB

1.2.2 Readout/Controls

Display
Four digit Nixie readout −180.0° to +360.0° with automatic lead-lag (+ and −) indication.

Phase Ranges
Selected . . . . . 0/360°
Selected . . . . . −180°/+180°

NOTE
Phase measurements within 5° of Range Limit —Not specified.

Auto Range . . . . . 0°/360 or −180°/+180°

NOTE
Unit will auto range within approximately 10 to 20 degrees of range limit.

1.2.3 Analog (Recorder Output)

OUTPUT −10 mV/DEG
Amplitude, 0°/360° Range . . . 0 Vdc to −3.600 Vdc
Amplitude, −180°/+180° Range. .+1.8 Vdc to −1.8 Vdc
Output Impedance . . . . . 1 kΩ

BCD OUTPUT
Logic 1 . . . . . +2.4 V minimum
Logic 0 . . . . . +0.4 V maximum
Output Coding. 8-4-2-1

1.2.4 Response Time (Full Scale Change)

Analog
Less than 4 seconds

Digitizing Time
1 second maximum

Auto-Ranging
2 seconds

1.2.5 Programming Controls

Read Command Input
Accepts negative going pulse 2-10 V, 100 nanoseconds minimum width. Continuous read command available with rear panel switch.

Print Command Output
Pulse 0(±.4 V) to 2.4 V nominal when reading is available. Minimum width 50 microseconds.

All phase angle measurements are dependent on type of waveform, amplitude, and frequency. The diagrams below show the absolute accuracy, taking into account all sources of error.

The term relative accuracy means the accuracy of difference in phase reading from one condition to another. For example, it is the accuracy of 1) repeatability, 2) comparison of readings among unknown signals with respect to a given signal, 3) phase deviation of input without regard to zero offset.

ABSOLUTE ACCURACY
40 Hz-100 kHz

ALL ACCURACIES STATED ARE ± DEGREES

CHANNEL A AMPLITUDE PERCENT OF FULL SCALE	.1%	1%	10%	100%
100%	2.4	1.5	0.7	0.4
10%	1.5	0.7	0.6	0.7
1%	0.7	1.0	0.7	1.5
.1%	1.5	0.7	1.5	2.4

CHANNEL B AMPLITUDE
PERCENT OF FULL SCALE

MULTIPLICATION FACTOR
AS A FUNCTION OF FREQUENCY

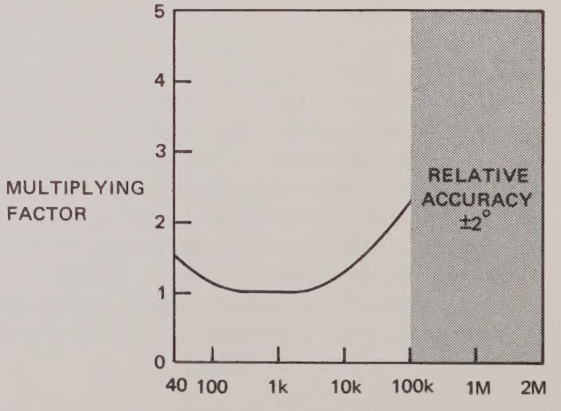


Figure 1.1. Instrument Accuracy Diagrams

1.3 SPECIFICATIONS GENERAL

1.3.1 Environmental Characteristics (Specifications Apply)

Recommended Warmup	30 minutes
Temperature	20°C to 30°C
Relative Humidity	30% to 75%

1.3.2 Mechanical

Dimensions
19 inches wide, 3-½ inches high, 16-½ inches deep.

Weight
14 lb. net, 24 lb. shipping

Power Requirements
105 – 125 Vac or 200 – 250 Vac, 50 Hz to 400 Hz less than 25 watts.

Connector:
BCD Output – Amphenol 57-40360
Input – BNC (female)
Mating Connectors:
BCD Output – Amphenol 57-30360
Input – BNC (male)

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_11283

SECTION 2
INSTALLATION AND OPERATION

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect the external parts for damage to switches, indicators, connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

The front panel has been designed to allow this unit to be mounted in a standard 19-inch equipment rack. No mechanical installation is required when the instrument is to be used as a portable bench unit.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

Connect the ac line cord to the mating connector at the rear of the unit and to the ac line supply. Check that the proper type of fuse is installed for the line supply being used.

NOTICE

Unless otherwise specified at the time of purchase, all Wavetek instruments are shipped from the factory with the power transformer connected for operation on a nominal 115-volt ac line supply, and a ½ amp 115 V line fuse.

NOTICE

Conversion for 230-volt operation requires resetting the 115/230 conversion switch at the rear of the instrument. Set the slide switch to 230, and install a fuse with a rating of ¼ amp at 230 volts.

2.2.2 Input Connections

Connect the desired input signals to their respective connectors using shielded cable equipped with female BNC connectors. Connect single-ended inputs to the appropriate polarity BNC, with the grounding cap on the opposite polarity BNC. Connect differential inputs between the "+" and "—" BNC, and disconnect the grounding cap. See Table 2-1 for input connections and there requirements.

Table 2-1. ELECTRICAL INSTALLATION GUIDE

Symbol	Name	Function	
J1	(Line Cord)	Connector for 3-wire line cord.	
J2	BCD Output	BCD Output Connector (See Table 2-2).	
J3	Input A "+"	Connectors for single-ended or differential input signal. The grounding cap is used only with single-ended input.	Observe amplitude specifications and limits of paragraph 1.2.
J4	Input A "—"		
J5	Input B "+"	Connectors for single-ended or differential input signal. The grounding cap is used only with single-ended input.	Use shielded cables with BNC connectors for these connections
J6	Input B "—"		

TABLE 2-2 MODEL 755 BCD OUTPUT CONNECTOR PIN LOCATION

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	2	4	8	1	2	4	8	1	2	4	8	1	2	±	READ COMMAND IN	RECORDER OUTPUT	CIRCUIT GROUD	PRINT COMMAND OUT	RANGE PROGRAM	RANGE MINIMUM CALIBRATE	RANGE MAXIMUM CALIBRATE	CHANNEL 'A' AMPLITUDE PROGRAM	CHANNEL 'B' AMPLITUDE PROGRAM
TENTHS				UNITS				TENS				HUNDREDS											

Pin No. Description

1-14 BCD OUTPUT — Logic 1 = +2.4 V minimum. Logic 0 = +0.4 V maximum 8421 output code

15 ± Indicating the signal on Channel B is leading the signal on Channel A for (+) and lagging the signal on Channel A for (−).
+ = +2.4 V minimum
− = +0.4 V maximum

16 READ COMMAND IN — When a negative going pulse of 2 to 10 volts and a minimum width of 100 nanoseconds is applied to this pin; the system will update its reading if in the external read command mode.

17 RECORDER OUTPUT — A dc voltage proportional to the phase reading is available between this pin and CIRCUIT GROUND pin (18).
−10 mV/degree from 1 kΩ impedance.

18 CIRCUIT GROUND — Reference for all program voltages and dc output.

19 PRINT COMMAND OUT — A pulse of 2.4 volts nominal with a minimum width of 50 microseconds will be applied to this pin when the BCD data is available.

Pin No. Description

20 RANGE PROGRAM — This function allows the programming of the phase range, either 0/360° or −180°/+180° range, if the AUTO RANGE/RANGE SELECT is in the RANGE SELECT position and the 0/360° −180°/+180° or EXT PROGRAM is in the −180°/+180° or EXT PROGRAM position. An open or 0 volt ±0.4 volt will place the instrument in the −180°/+180° range. A +2.4 volts will place the instrument in the 0/360° range. Voltages are referenced to CIRCUIT GROUND pin (18).

21 RANGE MINIMUM CALIBRATE — This selects the minimum phase detector range extreme, either −180° or 0°, to appear on the display and BCD OUTPUT so the phase detector and digital readout calibration can be checked. An open or +2.4 volts will inhibit this mode. A CIRCUIT GROUND pin (18) ±0.4 volts will select this calibrate mode. The voltages are referenced to the CIRCUIT GROUND pin (18).

22 RANGE MAXIMUM CALIBRATE — This selects the maximum phase detector range extreme, either +180° or 360°, to appear on the display and BCD OUTPUT so the phase detector and digital readout calibration can be checked. An open or +2.4 volts will inhibit this mode. A CIRCUIT GROUND pin (18) ±0.4 volts will select this calibrate mode.

Pin No. Description

23 CHANNEL A AMPLITUDE PROGRAM – Allows the selection of one of two ranges. An open or +2.4 volts allows .003 to 300 volts rms input sensitivity. A CIRCUIT GROUND pin (18) ±0.4 volts allows .001 to 2 volts rms input sensitivity. The voltages are referenced to the CIRCUIT GROUND pin (18).

24 CHANNEL B AMPLITUDE PROGRAM – Allows the selection of one or two ranges. An open or +2.4 volts allows .003 to 300 volts rms input sensitivity. A CIRCUIT GROUND pin (18) ±0.4 volts allows .001 to 2 volts rms input sensitivity. The voltages are referenced to the CIRCUIT GROUND pin (18).

2.3 OPERATING CONTROLS

The operating controls and electrical connections for the Model 755 rear panel are shown in Figure 2-1. The listing below discusses each control and its function.

1. **115/230 CONVERSION SWITCH** – Converts the power transformer to be used with either 115 Vac or 230 Vac.

2. **FUSE** – ½ amp to 115 Vac, ¼ amp for 230 Vac.

3. **BCD OUTPUT CONNECTOR** – A digital output representing the phase angle between the two inputs. See Table 2-2 for input and output programming connections and associated interface information.

4. **CALIBRATE SWITCH** – Used for quick check of phase detector calibration and digital offset.

5. **0/360 – 180/+180 or EXT PROGRAM** – This switch allows manual selection of phase range limits. When in the 0/360 position the Model 755 is in the 0° to 360° phase range. When in the −180/+180 or EXT PROGRAM position the Model 755 is in the −180° to +180° phase range or externally programmable, which allows the phase range to be changed by an external signal applied to the appropriate pin on the BCD connector (See Table 2-2).

6. **AUTO RANGE/RANGE SELECT** – In the AUTO RANGE position the Model 755 automatically changes its phase range as needed for a specific phase angle measurement. When in the AUTO RANGE mode the 0/360 −180/+180 range switch is deactivated. In the RANGE SELECT position the operator has the capability of manually selecting the range he desires.

7. **EXT READ COMMAND/CONTINUOUS READ** – In the EXT READ COMMAND position, an external read command pulse must be received at the BCD connector (See Table 2-2); which will allow the system to update its reading and give one print command. The instrument will hold the phase reading until another external print command is received, at which time it will update the reading and give another print command, when the data is available, on the BCD OUTPUT connector and the front panel display. In the CONTINUOUS READ position the

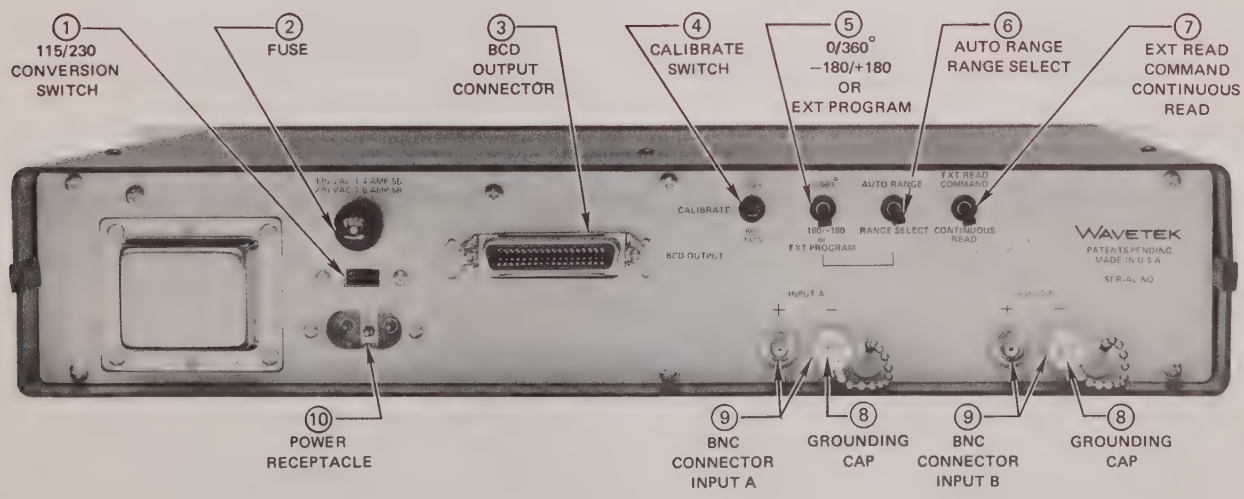


Figure 2-1. Operating Controls

instrument will continually update its reading every second and give a print out command upon each updating.

8. **GROUNDING CAPS** – Is a special BNC cap that shorts the connector to circuit ground.

9. **BNC CONNECTOR** – Input connectors for the signal source to be measured.

10. **POWER RECEPTACLE** – Connection for detachable line cord.

FRONT PANEL (not shown)

POWER – On/Off switch for power.

2.4 PRELIMINARY CHECKS

This paragraph outlines a quick bench checkout procedure for determining proper operation of the instrument. Field calibration and checkout instructions are given in Section 4 for determining if the unit is within all electrical specifications. No special test equipment is required to perform the checkout of the instrument as outlined below:

1. Connect the line cord to the instrument and the line supply, depress POWER pushbutton, and allow a 30 minute warmup period.

2. Position the rear panel switches as follows:
   0/360 –180/+180 or EXT PROGRAM to 0/360
   AUTO RANGE/RANGE SELECT to RANGE SELECT
   EXT READ COMMAND/CONTINUOUS READ to CONTINUOUS READ

3. Hold the CALIBRATE switch in the +360.0/+180.0 position. The readout should display "+360.0" ±000.2°.

4. Hold the CALIBRATE switch in the 000.0/–180.0 position. The readout should display "000.0" ±000.2°.

5. Change 0/360 –180/+180 or EXT PROGRAM switch to the –180/+180 position, and hold the CALIBRATE switch in the +360.0/+180.0 position. The readout should display "+180.0" ±000.2°.

6. Hold the CALIBRATE switch in the 000.0/–180.0 position. The readout display should read "–180.0". ±000.2°.

If, after sufficient warmup, the proper readings are not observed, refer to the Calibration Instructions given in Section 4 paragraph 4.2 of this manual.

2.5 OPERATION PROCEDURE

2.5.1 Phase Angle Measurement

To measure the phase angle between any two ac signals within the specified frequency and amplitude ranges, proceed as follows:

1. Set the EXT READ COMMAND/CONTINUOUS READ switch in the CONTINUOUS READ position.

2. Set the AUTO RANGE/RANGE SELECT switch in the AUTO RANGE position.

   NOTE

   The 0/360 –180/+180 switch is deactivated in this mode.

3. Program the appropriate amplitude range (with no programming the instrument is in the .003 V to 300 V range).

4. Connect one ac signal to INPUT A and the other signal to INPUT B.

N O T I C E

If single-ended ac inputs are used, the grounding cap must be connected to the unused input BNC. If differential ac inputs are used, the grounding caps must be removed and the input signal must be connected between the positive and negative (+ and –) BNC.

If the readout jumps or scatters occasionally with low input amplitude and/or frequency, it is probably caused by noise spikes riding on the input signal or a high signal to noise ratio. To eliminate or reduce this effect, connect a 0.1 μF capacitor (or matched filters) across input terminals.

N O T I C E

---

5. Read phase angle (phase difference) directly on digital display. If the readout polarity is positive, INPUT B leads INPUT A by the measured number of degrees. If the readout polarity is negative, INPUT B lags INPUT A by the measured amount.

6. The BCD OUTPUT provides the same data, electronically, for use as a control signal or for general recording applications.

7. For system operation, the Phase Range, Amplitude Range, and Range Calibrate pins may be externally programmed and the External Read Command feature may be utilized as specified in the BCD OUTPUT connector (See Table 2-2).

SECTION 3
CIRCUIT DESCRIPTION

3.1 SIMPLIFIED BLOCK DIAGRAM

As shown in Figure 3-1, the Model 755 Programmable Phase Meter consists of two similar input channels (only the A channel has the 0/360 −180/+180 selector switch) and a common output channel. Paragraph 3.2 provides further descriptions of the functions of each basic circuit comprising this instrument. This paragraph describes, briefly, the major circuit elements and their relationship to one another.

The Frequency Compensated Attenuator in each input channel is used to reduce high amplitude inputs to a level suitable for the remaining circuitry.

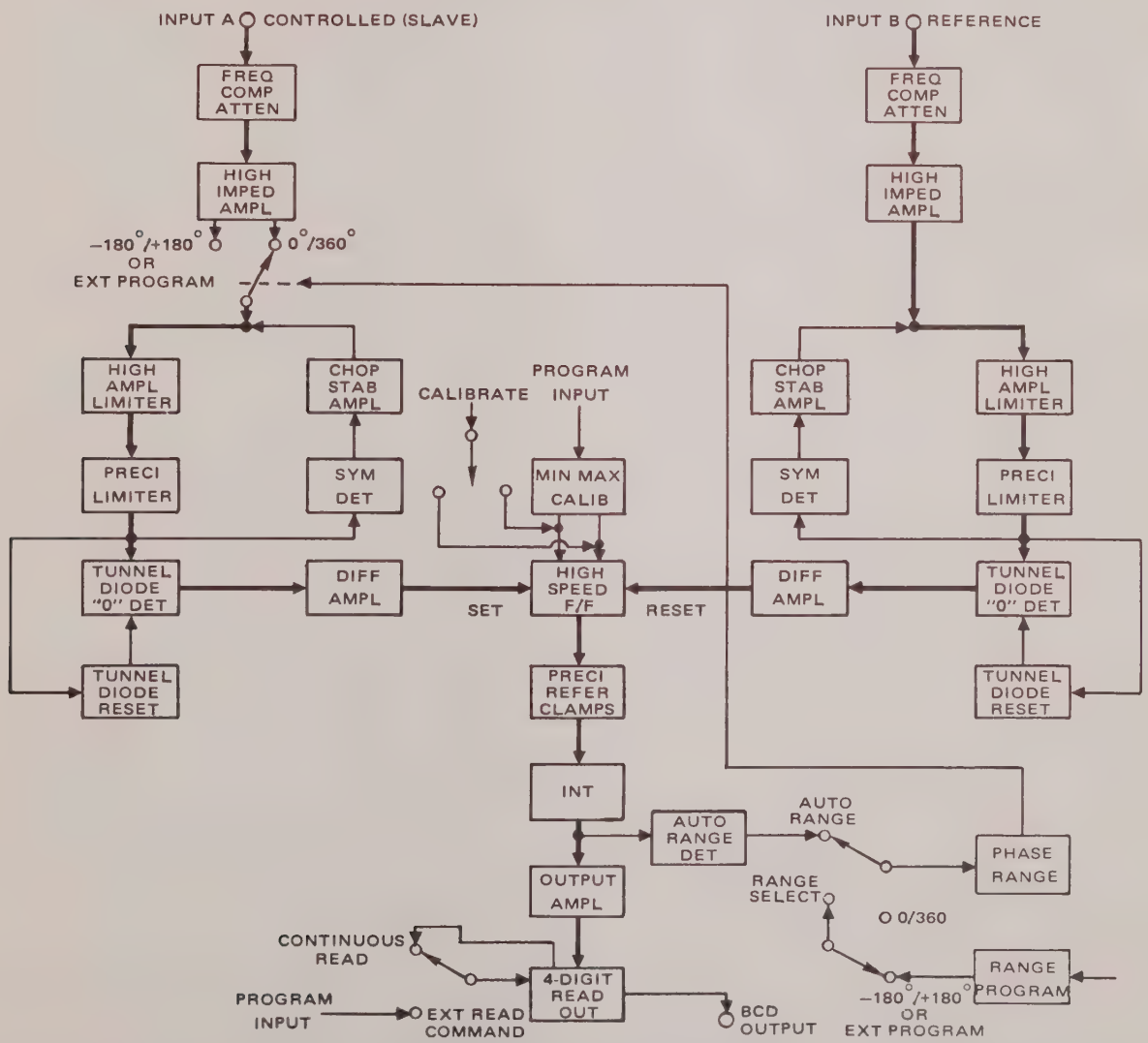


Figure 3-1. Simplified Block Diagram

The selected input signal is applied, through a High Impedance Attenuator, to a High Impedance Amplifier stage. In the A channel, the 0/360 −180/+180 or EXT PROGRAM switch select the appropriate phase out of the differential amplifier. The B channel does not employ a 180° phase shifter, as only one is needed in the instrument. Another function of the High Impedance Amplifier is to isolate the plus and minus inputs and provide high common mode rejection.

Next, the signal is high-amplitude-limited to prevent overdriving in the Precision Limiter stage. The Precision Limiter is a nonlinear feedback, wideband amplifier which limits the input signal at ±100 μV. The limited output signal is applied to a Symmetry Detector which integrates the waveform and produces a dc voltage that is proportional to the symmetry of the clipped waveform. This dc output represents an error in the zero-crossing system or an error due to the distortion of the input signal. The dc level is amplified and inverted in a Chopper Stabilized Amplifier and summed at the input to the first limiter stage. The closed-loop circuitry provides long-term, stable phase detection and automatically balances the limiters to correct for drift or offset voltages in the system due to temperature variations or component aging. Errors due to even-harmonic distortion are essentially eliminated by this self-balancing zero-crossing technique.

Following the limiters, the waveform zero-crossing is detected in a wideband Tunnel Diode Zero Detector. The Tunnel Diode Reset supplies the reset signal to the detector and provides system noise immunity. The detected zero-crossing output is then applied to the High Speed Flip-Flop through a Differentiating Amplifier. The output of Channel A is applied to the "set" input, and the output of Channel B is applied to the "reset" input of the flip-flop.

The flip-flop output is applied to a Precision Reference Clamp stage which provides a signal having an amplitude defined by the reference voltage and a duty cycle proportional to the phase difference between the two input signals. This output is integrated into a dc voltage proportional to the phase difference and is applied to the Output Amplifier for full scale and zero adjustment, before being applied to the digital display readout and output connectors.

The Range Maximum and/or Minimum calibrate programmable capability allows the instrument to select the maximum or minimum range, of the range selected, for presentation on the digital readout.

The Auto Ranging is only in the circuit when the AUTO RANGE switch is closed, through which the Auto Range Detector indicates to the Phase Range when either of the range extremes are approached. The Phase Range automatically changes to the appropriate phase range. During the transition, the digital readout is inhibited so that an erroneous reading is not presented to the BCD output during the change. The automatic ranging cycle takes approximately two seconds.

3.2 FUNCTIONAL BLOCK DIAGRAM ANALYSIS

As each functional circuit is described, refer to the appropriate block diagram and, if necessary, the appropriate portions of the schematic diagrams at the rear of this manual.

3.2.1 Zero Crossing Circuit

Both input channels employ similar Zero Crossing Circuits; the only difference being the RANGE switch in Channel A. In view of this, only the functions of Channel A are described, realizing that there are counterparts in Channel B. Figure 3-2 is a functional block diagram of the Zero Crossing Circuit, Figure 3-3 shows key waveforms within this circuit.

The input signal is passed through the amplitude programmable frequency compensated attenuator before being applied to Q1-Q2. The plus and minus inputs are symmetrically attenuated in the ac/dc attenuator which is adjusted for a flat frequency response by trimmer capacitors C1 and C5.

The input source currents for the High Impedance Differential Amplifier stage are balanced by trimmer adjust R187 to yield best common mode rejection. The output of Q1-Q2 is applied, through the selected RANGE switch, to either the positive or the negative input of Input Amplifier IC1.

Trimmer capacitors C10 and C11 adjust the phase shift of the negative and positive inputs to IC1 to match those of IC4 in Channel B for best high frequency performance. IC1 provides either a 180° or a 0° phase shift, depending on the setting of the RANGE selector switches. With either range the gain of IC1 is unity, and its output is applied to the summing junction at the gate of Q3. FET Q3 and transistor Q4 provide a high input impedance to the summing point, as well as temperature compensation. The output from Q3-Q4 is applied to the symmetrical Amplitude Limiter CR1-CR4. R21 is used to balance this four-diode limiter.

The output from CR1-CR4 is coupled to Precision Limiting Amplifier IC2, a 50 MHz amplifier with nonlinear feedback. R28 is a dc balance adjustment, C22 is a phase matching trimmer. The output of IC2 is a clipped waveform having an amplified volts/second relationship at the zero crossing of the input waveform.

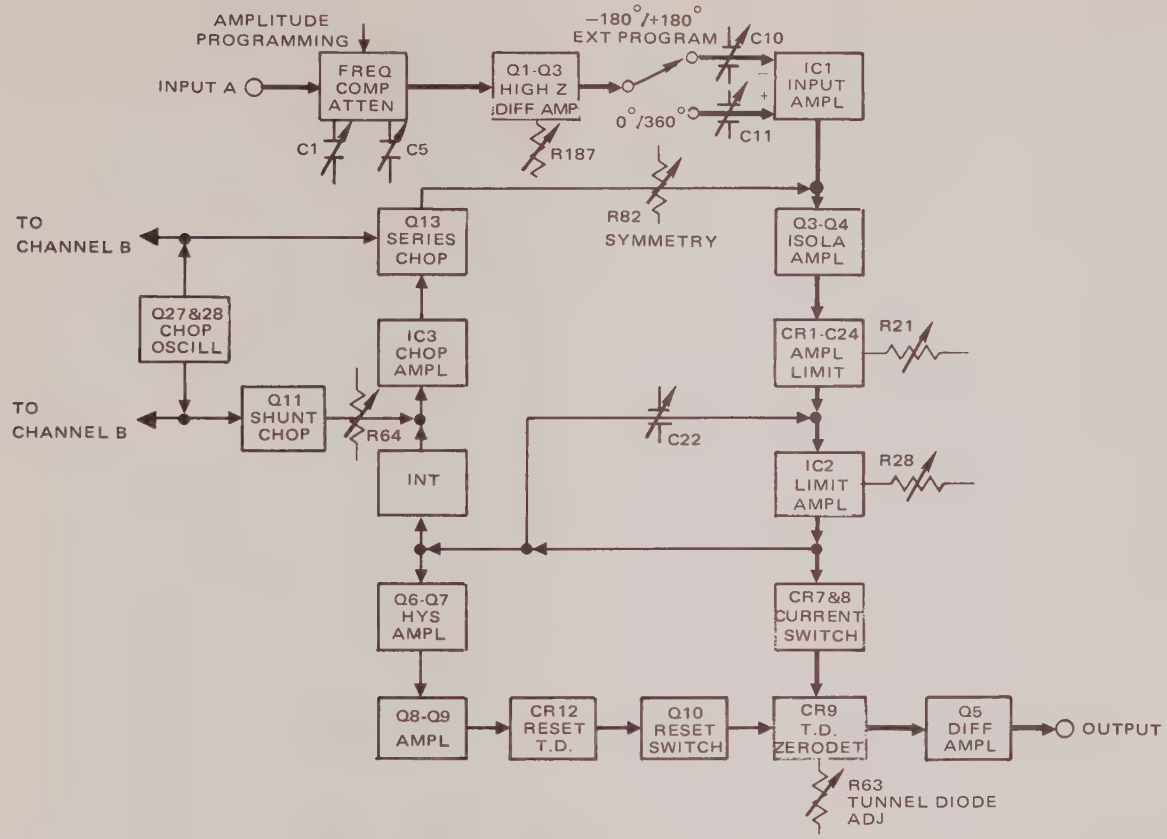
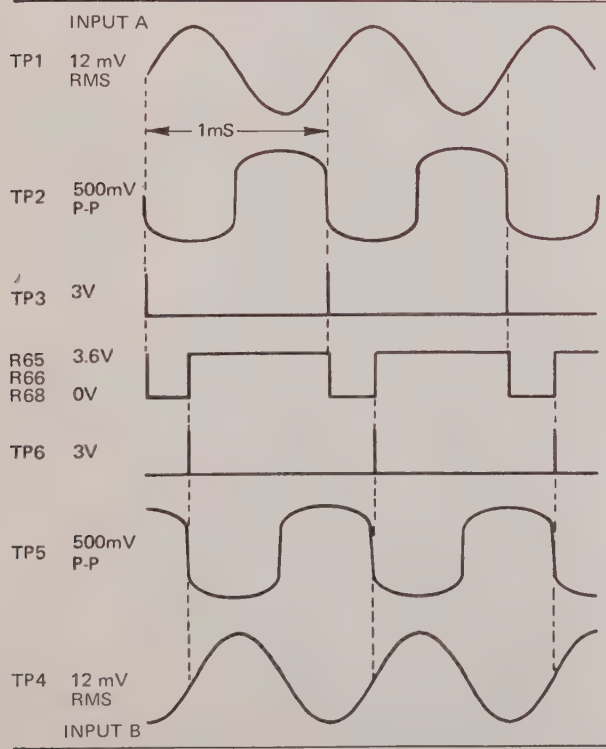


Figure 3-2. Zero Crossing Circuit, Functional Block Diagram



NOTES

PHASE RANGE 0/360°

INPUTS 10 mV RMS

CHANNEL B LAGS BY 90°

Figure 3-3.
Timing Diagram, Zero Crossing, and Logic Circuit

For high accuracy, the output of the final limiting amplifier of a zero crossing system must be symmetrical for a sine wave input. To ensure this, the output waveshape must be sampled periodically and the result fed back to the input of the first limiter to correct any unbalance or dissymmetry. The Integrator (comprised of R37-R40 and C26 and C30) supplies a dc voltage proportional to the symmetry of the output of IC2 to the input of Chopper Amplifier IC3. Shunt Chopper Q11 converts the dc output of the Integrator to an ac signal. R64 is the chopper balance adjust.

This ac signal is then amplified in IC3, and the output is demodulated in Series Chopper Q13. The voltage developed across capacitor C59 is an amplified error signal proportional to the nonsymmetry of the output of IC2. This error signal is applied, through R23, to the summing point at the gate of Q3. R82 is a symmetry adjustment which controls the amount of error signal in the feedback loop. This chopper-stabilized symmetry-detection system also eliminates the effects of even harmonic distortion with the limits of the chopper loop.

The symmetrical output of IC2 is then applied to Current Switch CR7-CR8 which supplies a small amount of current, at the actual zero crossing point, to trigger Tunnel Diode Zero Detector CR9. Tunnel Diode Adjust R63 sets the firing point of CR9 to be at the zero crossing point.

Differentiating Amplifier Q5 then supplies a pulse output which occurs at the true zero crossing point of the input waveform.

The reset circuitry for CR9 consists of transistors Q6 through Q10. Hysteresis Amplifier Q6-Q7 amplifies the output of IC2 and provides the necessary hysteresis to prevent double triggering. The output from Q6-Q7 is applied, through Amplifier Q8-Q9, to reset Tunnel Diode CR12. When CR12 fires, the resultant waveform is differentiated and drives Reset Switch Q10 to saturation which, in turn, resets the Tunnel Diode Zero Detector CR9 to its original state.

Chopper Oscillator Q27-Q28 is the circuitry common to both channels of the Zero Crossing Circuit. This oscillator supplies the chopper pulse which drives the gates of field-effect-transistors Q11 and Q13 at the proper sample rate.

3.2.2 Logic Circuit

The Logic Circuit converts the pulse information generated by the Zero Crossing Circuit into a precision, linear dc voltage whose value is a direct function of the phase difference between inputs A and B.

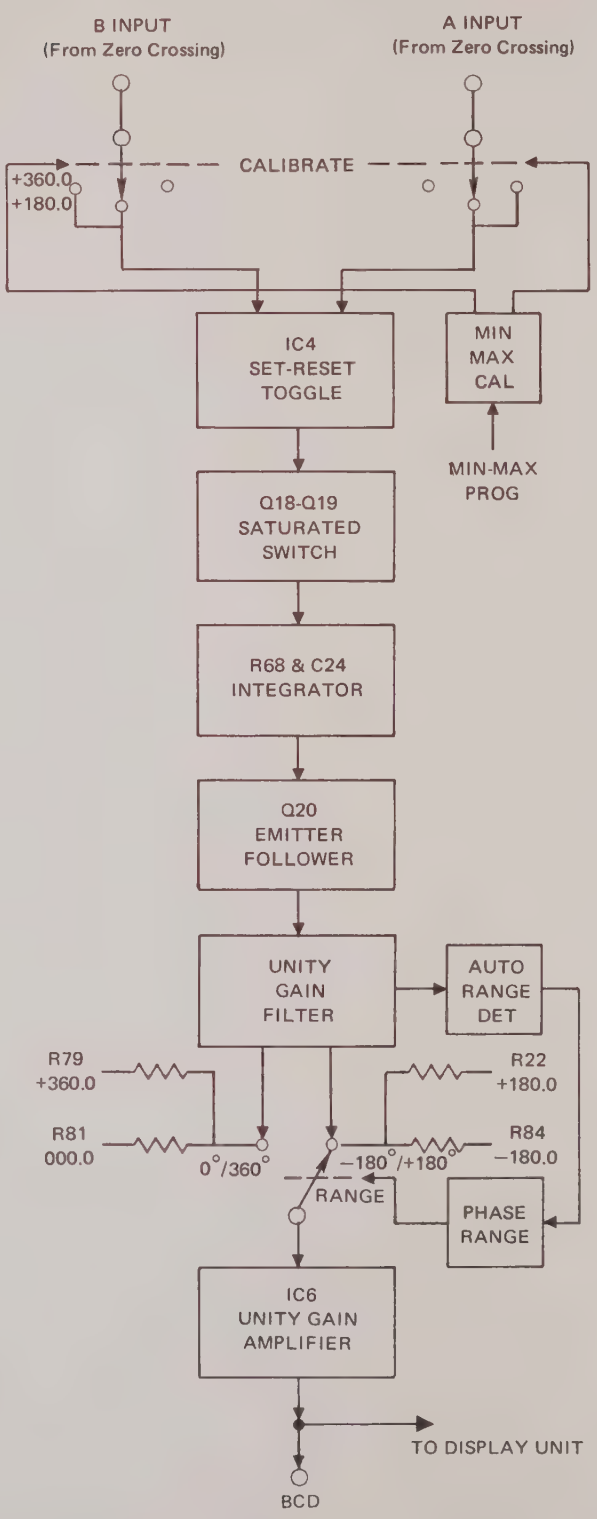


Figure 3-4. Logic Circuit, Functional Block Diagram

The two pulses generated by the Zero Crossing Circuit are applied to the inputs of a fast rise and fall time Set-Reset Toggle IC4. This stage is a dual transistor gate connected as an RS toggle with hot carrier diodes CR13 and CR14 providing nonsaturated, high speed operation. This stage converts the pulse information into a rectangular waveform that drives Saturated Switch Q18-Q19.

When the CALIBRATE switch is actuated, it inhibits either the "A" or "B" input from the Zero Crossing Circuit. With one input inhibited, the Set-Reset Toggle IC4 will go to a single state and remain. One state of IC4 corresponds to 0°, the other state corresponds to 360°. Therefore, when CALIBRATE switch SW3 is actuated, all dc calibrations may be checked.

Q18-Q19 operates as a pair of saturated switches between ground and a precision +3.6 Vdc. The resulting output, at the junction of R65 and R66, is integrated in Integrator R68/C24 and then filtered by an active Unity Gain Filter comprised of IC5, R69, R70, C25, and C26. Q20 functions as an Emitter Follower input to the Unity Gain Filter.

The integrated and filtered signal, representing the phase angle between INPUT A and INPUT B, is then conditioned in the Unity Gain Amplifier IC6. The final dc voltage out of IC6 has a −10 mV/degree relationship to the measured phase angle, and is provided (at J8) as an output as well as the input to the Digital Display Circuit.

RANGE calibration is accomplished by four potentiometers at the rear of the unit. When the 0°/360° RANGE is selected, the +360.0 and 000.0 limits may be calibrated using R79 and R81 respectively. When the −180°/+180° RANGE is selected, the +180.0 and the −180.0 limits may be calibrated using R22 and R84 respectively.

The reference voltage at the integrator input is the same voltage used as the voltmeter reference. The result is a ratio measurement that is independent of power supply drift.

3.2.3 Auto Range Circuit

Refer to the Auto Range Board Schematic at the rear of this manual when reading the following circuit description.

The filtered output of the Logic and Power Supply Board is applied to pin 13 of the Auto Range Board. The filter output is a dc voltage proportional to the phase shift between the inputs to the phase meter. This dc voltage is always between zero and 3.6 volts for 360 degrees. This dc voltage is then applied, through R13 and R14 to a dual comparator. The comparator has two reference voltages against which it compares the filter output. One is a positive reference voltage determined by R10 and R12, adjustable between zero and 1 volt approximately. This is the low level set point.

The high level set point is determined by R16 and R17, and can be set between 3 and 3.6 volts approximately. When the filter output approaches and equals either one of the set limit voltages, the output of the comparator (at pin 9 on Auto Range Board) makes a negative transition. This negative transition is coupled through C3 to toggle the JK flip-flop IC2 to the opposite state. The change of state of IC2 provides a signal at pin 7 which drives the range switch transistor Q2 and, in turn, drives the range change relays to the opposite range.

At the same time the negative transition toggles IC2, this negative transition is also applied to Q5 through R25. This inverts the pulse to a positive going pulse which triggers the single shot, IC3. IC3 has a two-second time constant such that when it is triggered pin 7 of this single shot drives Q4, through R23, and holds it in the conducting state. This action holds the junction of C3 and R24 to zero so that IC2 cannot make another transition until the range has been changed and the filter output (pin 13 of this board) has reached its steady state condition.

The relays for the auto ranging circuitry (K5, K6, K7, and K8) change the input phase shift of Channel A to add a 180 degree phase shift for the 0 to 360 degree mode. It also adds an opposing dc bias voltage in the phase detector circuitry so that the digital readout is compensated for the phase shift added to the input.

The programmable amplitude ranges are also located on the Auto Range Board. Q1 and Q3 are the relay drivers associated with the relays for Channel A and Channel B amplitude programming respectively. Relays K1, K2, K3, K4, K9, K10, K11 and K12 program the attenuators for Channel A and Channel B.

3.2.4 Minimum Maximum Calibrate

Refer to the Min/Max Calibrate Board Schematic at the rear of this manual when reading the following circuit description.

The two transistors Q16 and Q17 are relay drive transistors which when energized, actuate K12 and K13 relays. When pin 21, of the BCD output connector is grounded, transistor Q17 is energized; which is the closure on K13 relay. This places the system in the minimum calibration range mode displaying 000.0 or −180.0 on the front panel digital output and is also available at the BCD output connector. If pin 22, of the BCD output connector is grounded transistor Q16 is energized which provides the closure on relay K12. This places the system in the maximum calibration range mode.

This allows the maximum reading of the range selected, 360.0 or +180.0, to be presented on the front panel digital display and the BCD output connector.

3.2.5 Digital Display Circuits

The Digital Display Circuit is a four-digit, automatic-polarity-indicating, dual-slope-integrating, digital voltmeter (DVM). As this circuit is described, refer to the timing diagram (Figure 3-6) as well as the block diagram and schematic at the rear of this manual.

The −10 mV/degree dc output from the Logic Circuit is applied to the input of the Digital Display Circuit. This input is switched into an integrator for a precise time interval, causing the integrator to "ramp" to some voltage. At the end of the input time interval, a reference voltage is switched into the integrator causing it to ramp back to zero. The time between the start of the reference ramp and the time the reference ramp passes through zero is converted to a timing pulse by logic circuitry. The width of this pulse is directly related to the amplitude of the dc voltage input applied to the DVM, and thus, the phase relationship (phase angle) of INPUT A to INPUT B. This pulse is used to gate a counter so that, for each 1 mV of input voltage, one count is displayed, yielding .1° phase resolution on the digital readout.

The entire DVM is synchronized from a master clock, Oscillator IC7-Q17, which is called down in the four 10^n Decade Counters to provide the DVM time base. This time base controls the input to the Integrator, IC1, and sequences logic decisions used to generate the counter gating pulse.

The Integrator, IC1 and C2, has four inputs. The input voltage is switched in by Q1 and Q2. Depending on the input voltage polarity, either the +3.6 V reference is switched in by Q3 and Q4, or the −3.6 V reference is switched in by Q5 and Q6. Zero adjustment is made by R11 (ZERO OFFSET ADJ) which compensates for the input switch and integrator offset voltages.

It should be noted here that the +3.6 V used as the DVM reference is also the +3.6 V used to power the circuitry generating the dc output from the Logic Circuit. Thus, if the +3.6 V should change, there will be virtually no variation in the DVM output since a ratio relationship exists between the generating source and the measuring system.

The output of IC1 is detected in Comparator IC2 and the Amplifier comprised of Q8-Q10. IC3A and IC4A provide additional drive for the comparator input at zero, through Q7 and Q11, to prevent multiple comparator outputs. The amplified comparator output steers JK Flip-Flop IC5A which, upon receipt of the 10^{-3} 8 clock signal from IC5B, determines the polarity of the DVM input voltage. Once the polarity has been determined, either IC3B or IC4C changes state to switch in the appropriate reference voltage for ramping the integrator back to zero. As the reference voltage is switched in, IC3C is gated positive, producing the start of the output pulse. When the Integrator reaches zero, the Comparator changes state. This change in state causes IC3B or IC4C to gate IC3C negative, generating the end of the output pulse.

In the digital readout system, the analog board converts the dc output of the phase meter to a positive pulse whose width is proportional to the phase shift at the input to the instrument. This pulse is then applied to pin 4 of the Digital Readout Board.

The positive pulse is fed through R3 to the base of Q2, an inverter, causing the collector of Q2 to go negative for the same duration. The first negative transition of the pulse at the collector of Q2, coupled through C1, causes the output of IC2 to go positive. This positive output is applied to the reset pins of IC5, IC8, IC11, and IC14—the counter portion of the digital readout system. Thus, the negative transition of the pulse at the collector of Q2 causes a zero state to be set into the counter.

The clock input, a frequency of approximately 50 kHz, is applied through Q1 to pin 14 of IC5, the first decade of the decade counter stages. This frequency is then counted until a positive transition of Q2 is coupled through C2 causing IC2 to go negative. The single-shot configuration of IC2 provides a positive pulse at pin 8. This also drives pin 1 of IC1 to a positive condition which (if pins 8 and 11 of IC1 are in the reset condition) allows the pulse to get through to pin 3 of IC1 and pin 6 of IC1 to go negative. This action strobes the information from the clock decade counters into the latch circuits of IC4, IC7, IC10, and IC13, and also strobes the Print Command output circuit.

When the new information is updated into the quad latch circuitry, decoder drivers IC3, IC6, and IC9, and IC12 then decode the information and present it to the digital display tubes V1, V2, V3, and V4.

Another feature incorporated in the Digital Readout Board is the external read command. The external read command is an input through pin A6 which after passing through an isolation transformer T1 sets pin 11 of IC1 to a low condition when pin A6 is positive and when the rear panel switch is in the external read command position. When A6 is held positive, pin 11 is held at ground inhibiting the

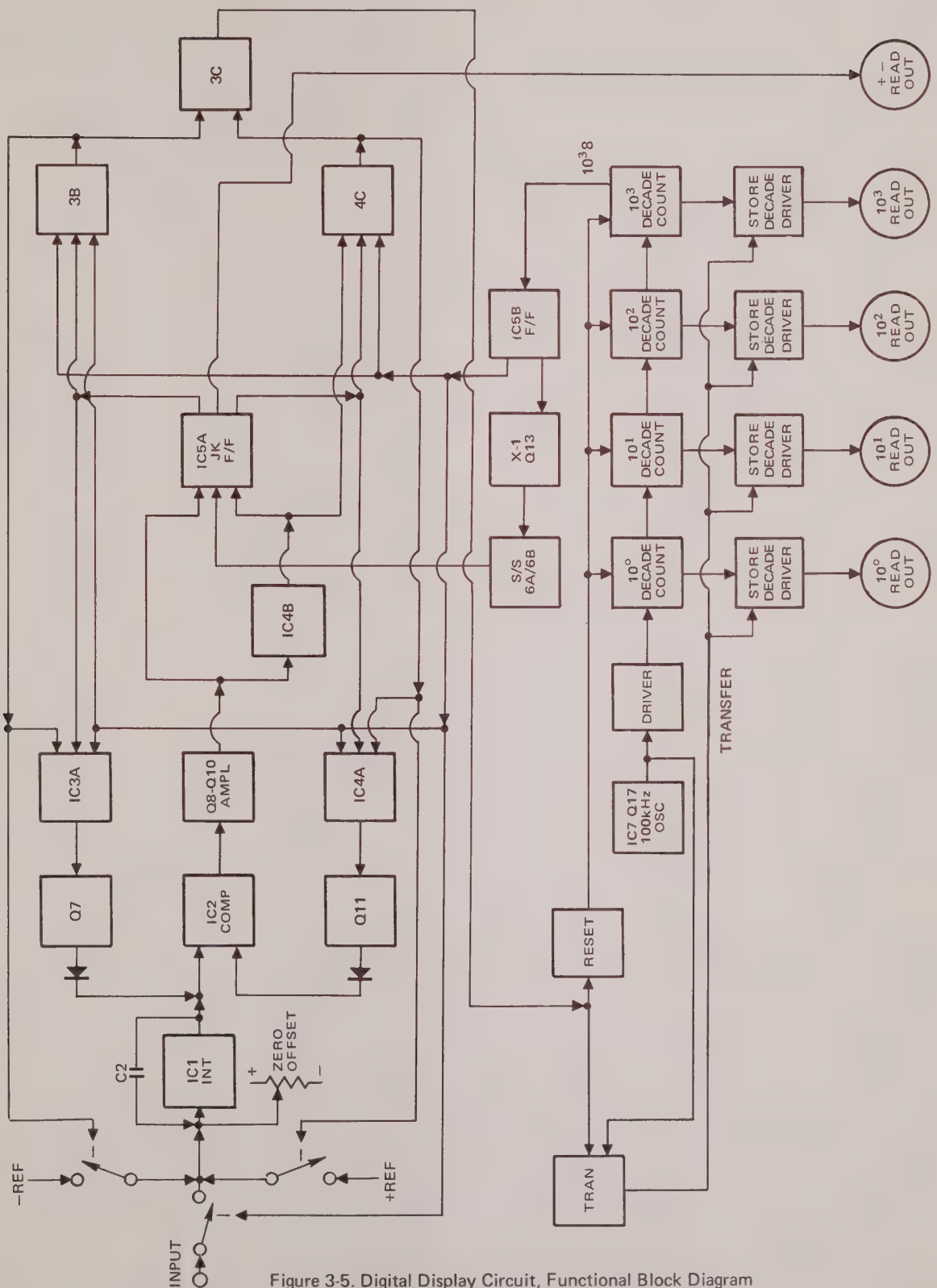


Figure 3-5. Digital Display Circuit, Functional Block Diagram

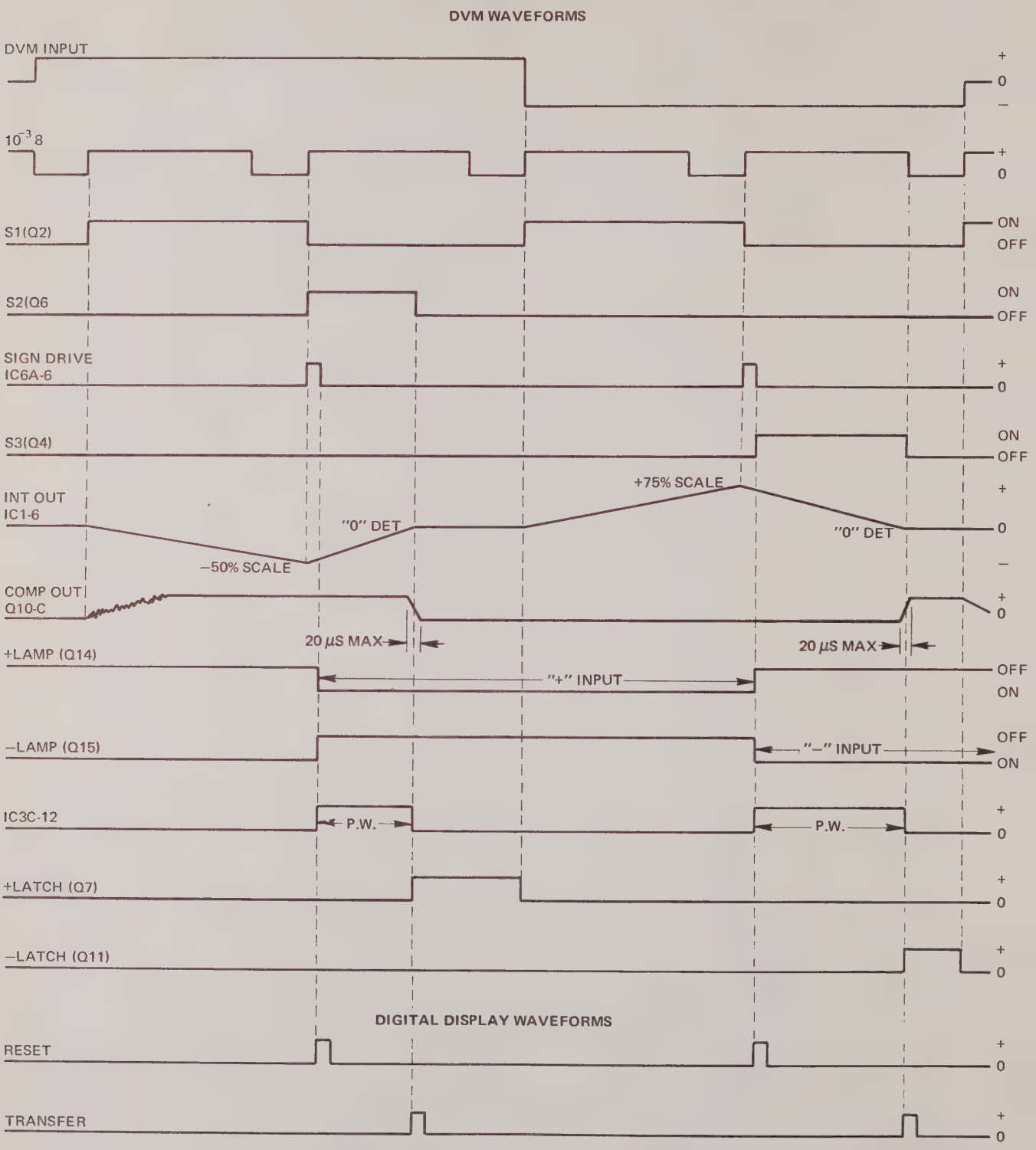


Figure 3-6. Digital Display Circuit, Timing Diagram

clock input at pin 2 of IC1. This action, in turn, inhibits the transfer command from the decade counters to the quad latch circuits. The print inhibit signal applied to pin 13 of IC2 inhibits the digital readout print command from external sources. In the normal Model 755 configuration, the auto range circuitry inhibits the digital readout during its transition period with this line.

Transistors Q3 and Q4 are the plus and minus sign drivers for the digital display tubes.

3.2.6 DC Power Supplies

Regulated operating voltages for the Model 755 Programmable Phase Meter include +15 V, −15 V, +3.6 V, −3.6 V, +5 V, and +180 V. AC line voltage is connected through the line cord to the POWER switch on the front panel. A slo-blo fuse is installed on the line side of the switch, and a 115/230 power selector switch connects the primary winding of the power transformer for the appropriate line voltage.

AC voltage is coupled from the transformer secondary to the bridgerectifier CR1-CR4. Filtering is provided by C3 and C11. Q12 is operated as a Zener diode reference voltage for the −15 V supply. IC3 is a comparator differential amplifier. The Comparator drives a Darlington-connected Series Pass transistor pair, Q9 and Q11, used for added current gain. Q8 is also connected to operate as a Zener diode reference to provide a voltage level shift for the output of IC3. R36, −15 V ADJ, adjusts the minus input of IC3 with respect to the plus input which has a Zener voltage of approximately 7 volts. If the −15 V tries to increase due to a change in line voltage or load current, the collector of Q12 stays approximately at the same voltage. Thus, the minus input to IC3 becomes more positive than the plus input, and the IC3 output draws more

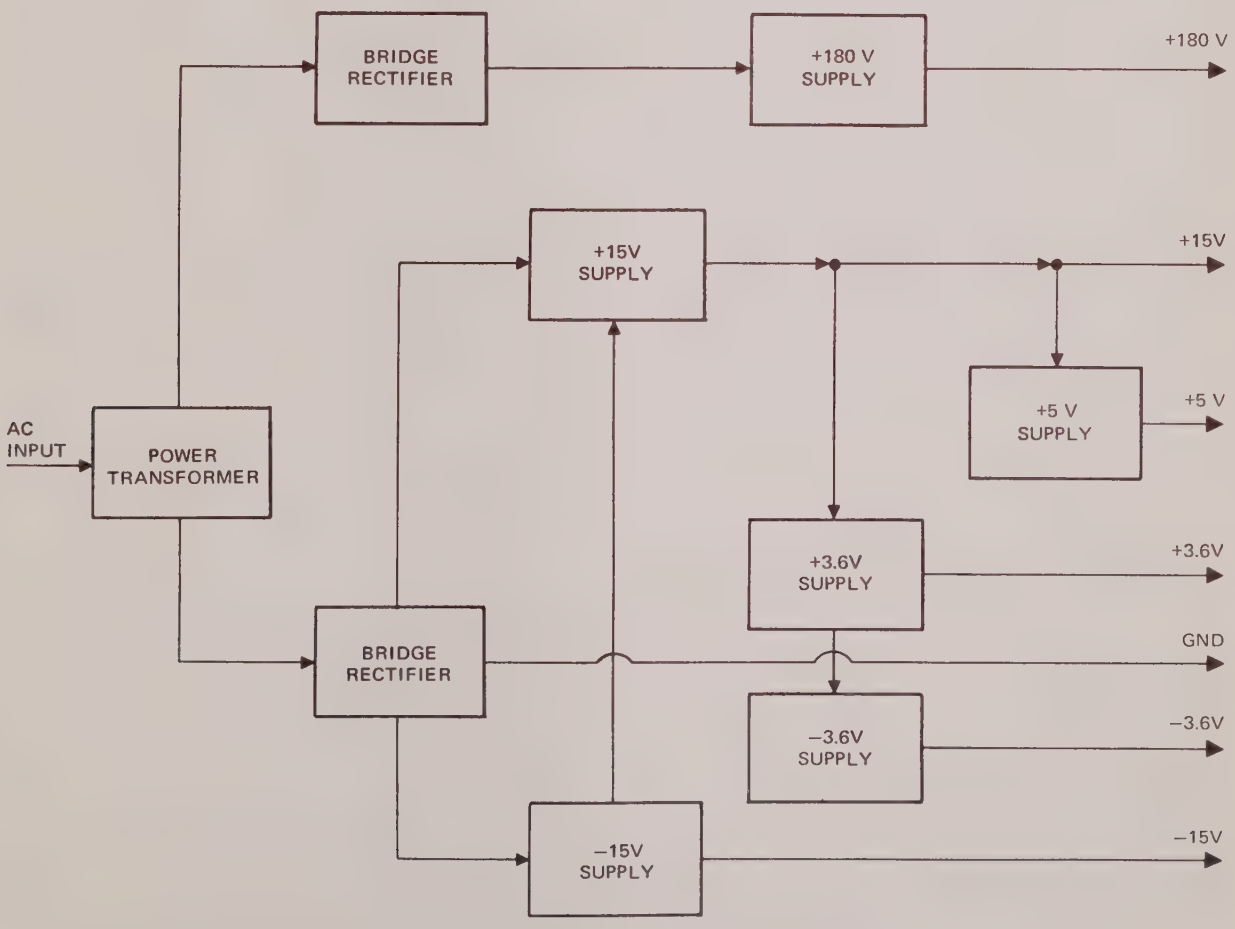


Figure 3-7. DC Power Supplies, Functional Block Diagram

current. The output moves less positive, and this change is coupled to the base of Q9 and Q11 through Q8, returning the supply to −15 volts.

IC1 is a Comparator Differential Amplifier in the +15 V supply. The plus input of IC1 is returned to ground through R9. Voltage Divider R7-R8, between the plus and minus 15-volt supplies, sets the minus input of IC1 precisely at ground. An increase in the −15 volts, due to line voltage variation or load current change, results in the minus input of IC1 moving positive, and the output of IC1 moving negative. This change is coupled to the bases of Q1 and Q2 through Q4. Q1 and Q2 form a Darlington-connected Series Pass pair for added current gain. The negative-going change returns the output to +15 volts.

Q3, in conjunction with R2 through R4, comprises a foldback current limiter for the +15 V regulator. Normally, the base of Q3 is turned off. Thus, the base of Q2 moves freely as the output from IC1 changes. When the +15 volt output is overloaded, heavy current flows through R2 and creates a potential drop across the resistor. When the potential drop overcomes the drop across R3, Q3 begins to conduct, starting to short the base of Q2 to the +15 volt output. In this condition, the output can be shorted indefinitely at a lower than maximum power dissipation of Q1. When the overload condition is removed from the +15 V output, the base of Q2 starts to rise. As the emitter of Q1 rises toward +15 volts, Voltage Divider R3-R4 has more effect on the base of Q3 and eventually turns Q3 off completely. When Q3 turns off, the normal condition is restored. Q10 with R28, R29, and R30, form a foldback current limiter for the −15 volt regulator.

The +3.6 volt supply is provided by Q5 and Q6 operating as a Comparator Differential Amplifier controlling the Series Pass transistor Q7. The error signal is obtained from the wiper of R20, in a Voltage Divider comprised of R18, R20, and R21 between +3.6 volts and −15 volts (the −15 volts here acts as a reference voltage) and R2 is used as the +3.6 volt adjustment.

The −3.6 volt supply is provided by IC2 operating as a Unit Gain Operational Amplifier with R22 providing gain control and the −3.6 volt adjustment.

For the +5 volt supply, ac voltage is coupled from the transformer secondary to Bridge Rectifier CR8-CR11. Filtering is provided by C14. Q14, Q15, and Q16 form a Comparator Differential Amplifier controlling Series Pass transistor Q13. The error signal is sensed directly on the +5 volts and is applied to the base of Q16. The Voltage Divider R38-R44, between +15 volts and ground, provides the reference voltage for the base of Q15. Q17, R40, R41, R42, and R43 form a foldback current limiter for the +5 volt regular.

For the +180 volt supply, ac voltage is coupled from the transformer secondary to Rectifier CR12. Current limiting is provided by R48 and filtering is provided by C17. R49 is a bleeder resistor for C17, to prevent a sustained high voltage after power is turned off.

3.3 SUPPLEMENTAL CIRCUITS

There are no unique or supplemental circuits within the Model 755 to be separately described as "Supplemental Circuits". The preceding circuit descriptions adequately describe the complete circuitry of the Model 755 to the degree required by a competent technician.

SECTION 4
MAINTENANCE

4.1 ACCESS INSTRUCTIONS

Removal of the dust cover affords quick access to the majority of components within the unit. However, it may be necessary to remove the Digital Readout Assembly or the Zero Crossing Board in order to gain access to those components not exposed by removing the dust cover. Instructions for all three are given below.

4.1.1 Removing the Dust Cover

1. Unplug the power cord.
2. Unscrew three captive screws on top cover.
3. Remove top cover.
4. Follow same procedure for bottom cover removal.

4.1.2 Removing the Digital Readout Assembly

1. Remove the two Phillips screws on top of the Digital Readout Assembly closest to the front panel.
2. Remove the two Phillips screws holding the two bars extending from the assembly to the rear panel.
3. The assembly can now be removed and placed on a support resting on two side plates. The unit may be turned on and operated while in this stage of disassembly.
4. Disconnect the connector pins.

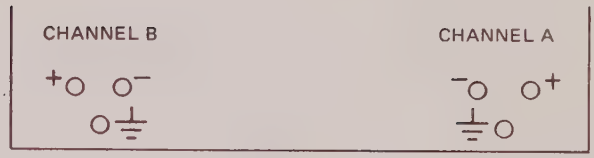
4.1.3 Removing the Zero Crossing Board

1. Place instrument on its top.
2. Remove bottom cover.
3. Remove the three bottom screws on both sides of the instrument holding the Zero Crossing Board to the side plates.
4. Disconnect the connector pins on front of instrument.

NOTE

The inputs are now available at the connector pins on the front of the Zero Crossing Board.

5. To replace the Zero Crossing Board, reverse the above procedure. When reconnecting the input connector pins, follow the diagram below.



Component Side of Zero Crossing Board

4.2 CALIBRATION INSTRUCTIONS

This paragraph provides complete sequential calibration instructions for the Model 755 Phase Meter. The instructions are concise and are written for the experienced electronics technician or field engineer having a working knowledge of this type of instrumentation.

WAVETEK maintains a factory repair department for those customers not possessing the necessary test equipment or personnel to maintain this type of instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached. This will hasten turnaround time.

Test point and control locations necessary for calibration are given within this section unless a foldout illustration is required. In the latter instance, the foldout illustration will be found at the rear of the manual.

4.2.1 Recommended Test Equipment

The following test equipment (or equivalent) is recommended for this calibration procedure.

VCG/VCA Generator	Wavetek Model 136
Voltmeter	1 mV Resolution
Oscilloscope	with Dual Trace 10 mV Sensitivity Lissajous Capability

4.2.2 Preliminary Procedures

Before attempting to recalibrate this instrument, the user should read and understand the entire calibration procedure. This procedure should be performed in the sequence given, as should the steps within each segment.

1. Connect the Model 755 Phase Meter in the test set up illustrated in Figure 4-1[A].
2. Set POWER switch to ON, set RANGE selector for 0°/360°, continuous read, range select.
3. Allow a 30-minute warmup period before attempting to calibrate this instrument.

4.2.3 Full Scale Calibration Procedure

4. With equipment connect as shown in Figure 4-1 [A]; hold CALIBRATE switch down (000.0/−180.0) and adjust (R81) for 000.0 plus or minus 1/2-count.

NOTE

One-half count (1/20th of a degree) can be determined by interpolation of alternate readings. If display alternates between ±000.0 and +000.1, the indication may be averaged to give +000.05. Careful adjustment should yield a display of ±000.0 (±.1) after equipment warmup.

5. Hold CALIBRATE switch up (+360.0/+180.0) and adjust (R79) for a display centered between +359.9 and +360.0.
6. Set RANGE selector for −180°/+180°.
7. Hold CALIBRATE switch down (000.0/−180.0) and adjust (R84) for a display centered between −179.9 and −180.0.
8. Hold CALIBRATE switch up (+360.0/+180.0) and adjust (R22) for a display centered between +179.9 and +180.0.
9. Repeat steps 4 through 8 for best indications. If all four calibrations are not within the specified limits, refer to the Logic Board Calibration Procedure given in paragraph 4.2.4.

4.2.4 Logic Board Calibration Procedure

10. Remove the top dust cover from the Model 755 Phase Meter following the procedures outlined in paragraphs 4.1.1 and 4.1.2.

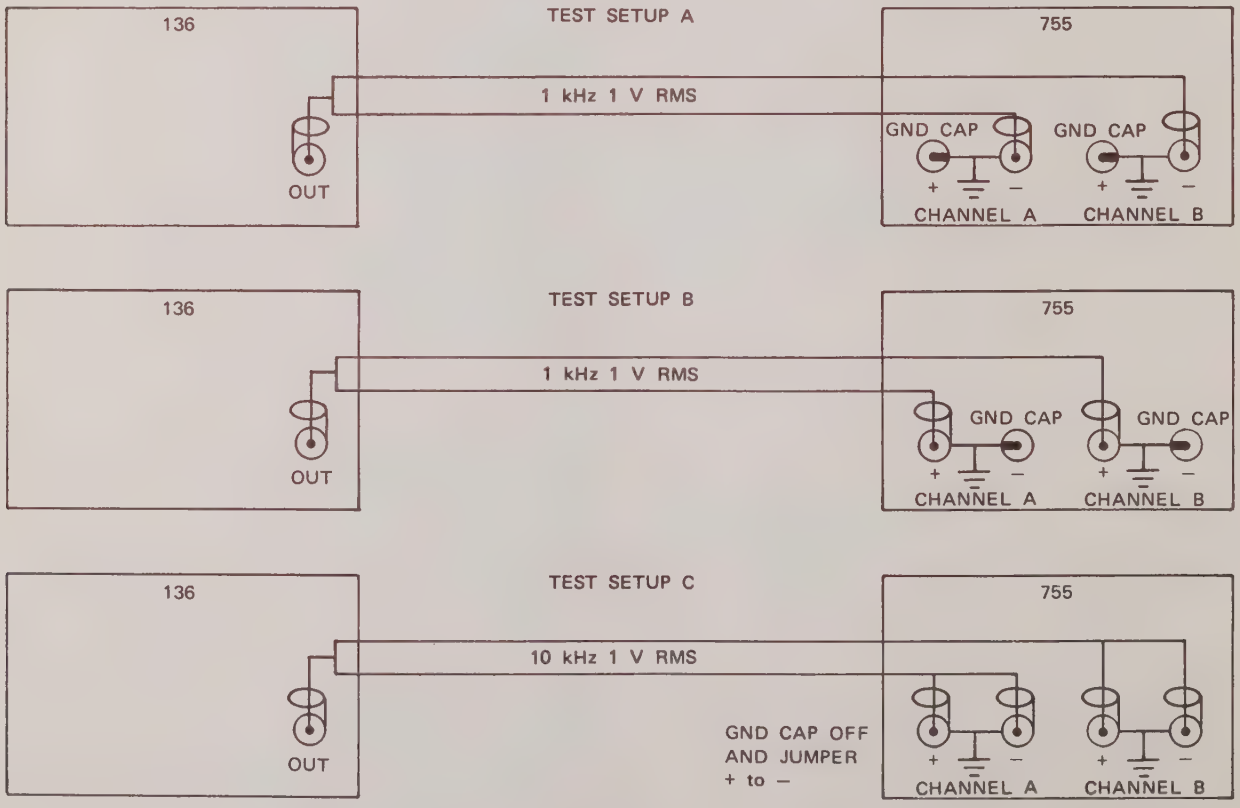


Figure 4-1. Calibration Set-up

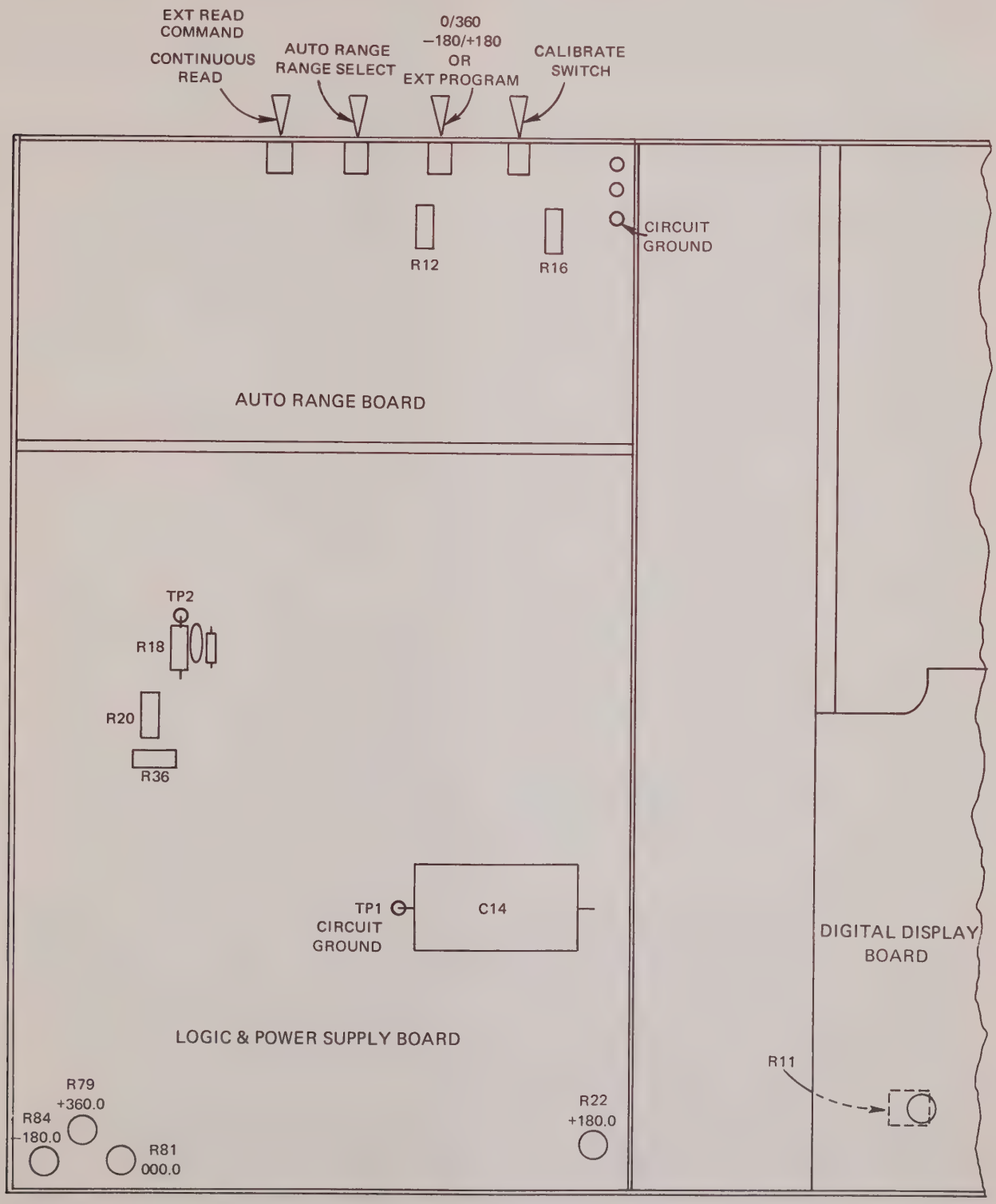


Figure 4-2. Calibration Locations on Logic, Auto Range and Digital Boards.

11. Connect the positive probe of the voltmeter to test point TP2, and the negative probe to TP1, of the Logic Board (Figure 4-2).
12. Set POWER switch to ON and allow a 30-minute warmup period.
13. Set RANGE selector to 0°/360°, and set (R20) to the center of its adjustable range.
14. Adjust (R36) to obtain +3.600 V (±2 mV between TP1 and TP2 (+3.6 V supply).
15. Connect the voltmeter to the Recorder Output at pin 17 on the BCD Output connector and circuit ground (TP1).
16. Hold CALIBRATE switch down (000.0/−180.0) and adjust (R81) for 0.000 V (±.3 mV) on the voltmeter.
17. Hold CALIBRATE switch down (000.0/−180.0) and adjust DIGITAL DISPLAY ZERO control R11 (accessible from the left side of the top printed circuit board of the Digital Display assembly) for a display of 000.0 plus or minus 1/2-count.
18. Hold CALIBRATE switch up (+360.0/+180.0) and adjust (R79) for a display centered between +359.9 and +360.0.
19. Hold CALIBRATE switch up (+360.0/+180.0) and adjust (R20) for −3.600 V (±.3 mV) on the voltmeter.
20. Set RANGE selector to −180°/+180°.
21. Hold CALIBRATE switch down (000.0/−180.0) and adjust (R84) for a display of −180.0 plus or minus 1/2-count. Voltmeter should read −1.800 V ±2 mV.
22. Hold CALIBRATE switch up (+360.0/+180.0) and adjust (R22) for a display of +180.0 plus or minus 1/2-count. Voltmeter should read −1.800 V ±2 mV.
23. If readings are within ±2 mV, turn power off and reinstall display.
24. If steps 16 through 22 are out more than ±2 mV on the voltmeter, repeat steps 14 through 22 again. If voltmeter still indicates readings outside the specified limits, refer to the Corrective Maintenance instructions in paragraph 4.3.

4.2.5 Zero-Crossing Mid-Frequency Procedure

25. Turn power on, and set RANGE selector to −180°/+180°. Program both VOLTS RMS to .001-2 V rms by applying a +0.4 volts to pins 23 and 24 of the BCD connector.
26. Connect a 1 kHz sine wave, 10 mV rms (28 mV p-p), into each input (Figure 4-1[A]).
27. Check 10:1 oscilloscope probe for dc zero, by connecting it to the circuit ground, and center trace on horizontal centerline of CRT. Set scope gain to 10 mV/cm, and sweep speed to 0.1 ms/cm.
28. Connect the scope probe to Channel A test point TP2 (Figure 4-3) of the Zero Crossing Board. The oscilloscope should display a waveform similar to the one shown in Figure 4-4[A].
29. Adjust DC BALANCE (R28) so that V_1 (Figure 4-4[A] is equal to V_2 (±10 mV).
30. Adjust CHOPPER BALANCE (R64) so that t_1 (Figure 4-4[A] is equal to t_2 (±1 μs).
31. Alternately perform steps 29 and 30 until the closest to optimum results are obtained.
32. Adjust TUNNEL DIODE (R63) until top of trigger is at zero volts dc (±1 mV) as shown in Figure 4-4[B].
33. Connect scope probe to test point TP5 adjust DC BALANCE (R119), CHOPPER BALANCE (R155), and Tunnel Diode (R154) and perform steps 29 through 32 for Channel B. Recheck oscilloscope for dc drift by connecting the scope probe to the phase meter ground and adjusting scope controls to reposition trace on horizontal center line.
34. If steps 25 through 33 have been followed correctly, the digital readout should indicate one half of plus and minus full scale (CALIBRATE switch up and down readings). This reading is called "out of case zero" in the rest of the manual.

Examples:

Calibrate "Up"	Calibrate "Down"	"Out of Case Zero"
+180.0	−180.0	000.0 (±.1°)
+180.2	−179.8	+000.2 (±.1°)
+180.2	−179.4	+000.4 (±.1°)

NOTICE

Do not be alarmed if the full scale values are not precise, the instrument is out of the case and will return to proper readings when case is replaced. It is important, however, that the "out of case zero" be displaced equally from the range extremes.

DO NOT READJUST
FULL SCALE VALUES AT THIS POINT

If "out of case zero" is not equally displaced repeat steps 25 through 33 and step 35 below. Go on to the Zero Crossing High Frequency Procedure; three or four tenths of a degree error could be caused by high frequency misalignment.

NOTICE

35. Increase the input signal amplitude to both channels to 1 V rms (2.8 V p-p). If reading changes more than ±0.1°, adjust PK-PK (R21) and (R112) for accurate time symmetry at test points 2 and 5, as shown in Figure 4-4[C].

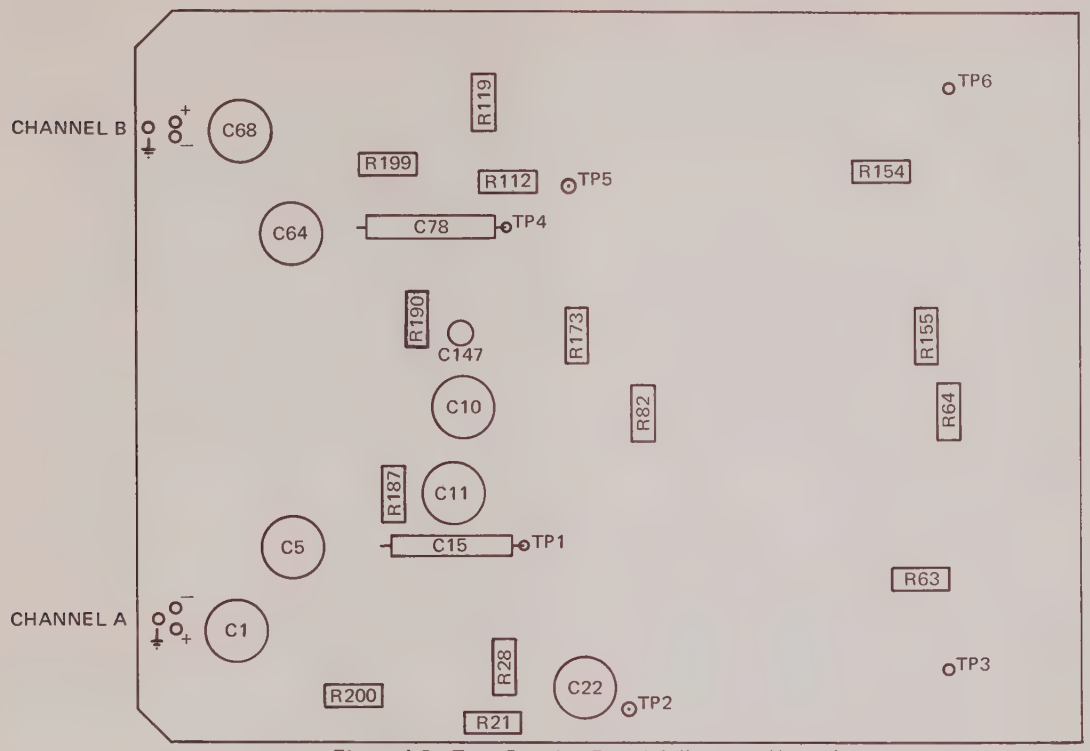


Figure 4-3. Zero Crossing Board Adjustment Locations

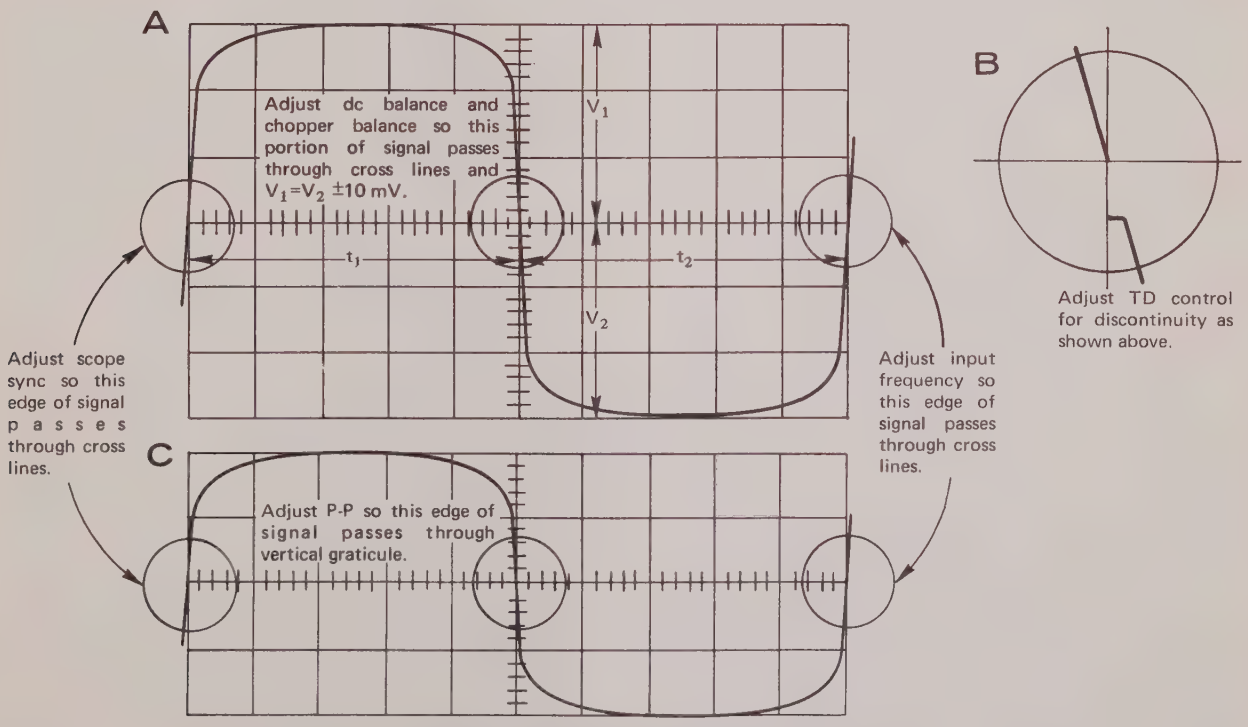

A
Adjust dc balance and chopper balance so this portion of signal passes through cross lines and $V_1=V_2$ ±10 mV.
V_1
V_2
t_1
t_2
B
Adjust TD control for discontinuity as shown above.
C
Adjust P-P so this edge of signal passes through vertical graticule.
Adjust scope sync so this edge of signal passes through cross lines.
Adjust input frequency so this edge of signal passes through cross lines.

Figure 4-4. Oscilloscope Calibration Displays

4.2.6 Zero-Crossing High-Frequency Procedure

36. Set RANGE selector to −180°/+180° and remove all scope probes.
37. Apply a 10 mV rms sine wave, 80 kHz, into both channels, using the test configuration shown in Figure 4-1[A].
38. Adjust C22 until digital readout is equally displaced from range extremes for "out of case zero" (±0.2).
39. Increase input amplitude to 100 mV rms, increase input frequency to 800 kHz, and adjust C10 until the digital readout equals "out of case zero" (±.4°).
40. Since steps 38 and 39 interact, they must be alternately performed until both readings, when going from one condition to the other, are within limits. Recheck steps 28 through 33 and, if necessary, readjust controls for proper indications.
41. Apply a 1 mV rms sine wave to both inputs, using the configuration shown in Figure 4-1[A] and, while watching the digital readout, vary the frequency from 1 kHz to 10 kHz. Record the reading at 1 kHz and the reading at 10 kHz. Determine the difference between the two readings, taking into account the polarities indicated, and record this as the "error span".

Examples:

1 kHz Readings	10 kHz Readings	Error Span
−000.2	+001.0	1.2°
+000.2	+001.1	.9°
−000.2	−000.8	.6°

42. Set input frequency back to 1 kHz at 1 mV rms and equally adjust Channel A TUNNEL DIODE (R63) and Channel B TUNNEL DIODE (R154) so that the digital display readout indicates one-third of the Error Span with a minus sign. (This would be −000.4° in the first example shown in step 41.)
43. Set input frequency to 10 kHz at 1 mV rms and display readout should indicate two-thirds of the Error Span with a plus sign. If the Error Span is not distributed one-third and two-thirds at 1 kHz and 10 kHz respectively, repeat steps 41 and 42.

4.2.6.1 ATTENUATOR FREQUENCY ADJUSTMENT

NOTE

Make sure the oscilloscope probes are properly compensated for lissajous operation. Check each probe with the scope calibrate signal, then connect both probes to the same signal and vary the frequency from 10 Hz to 1 MHz and make final adjustment for closed lissajous.

44. Set both VOLTS RMS ranges to .3-300 by applying +2.4 volts or logic 1 to pins 23 and 24 of BCD connector and apply a 1 kHz 7 V rms sine wave to the positive input terminals as shown in Figure 4-1[B]. Connect the probes of a dual channel scope, with lissajous capability, between the plus input terminal and test point TP1 of Channel A.
45. While varying the input frequency from 1 kHz to 10 kHz, adjust C1 for a closed lissajous.
46. Connect the scope probes to TP1 and TP4 of Channel B. Adjust C64 for a closed lissajous. The digital readout should now read within ±.2° of reading obtained with 100 Hz input (switch to 100 Hz without changing amplitude and check). If it doesn't, repeat steps 45 and 46 until the readout is within this limit.

4.2.6.2 COMMON MODE REJECTION CALIBRATION.

Channel B

47. Set both VOLTS RMS ranges to .001-2 V rms by applying a +0.4 volts or logic 0 to pins 23 and 24 of the BCD connector.
48. Apply a 10 kHz, 10 mV rms, sine wave to both inputs as shown in Figure 4-1[C].
49. Connect scope probe to test point TP5 and circuit ground, and alternately adjust R190 and C147 for minimum signal. Increase input to 1 V rms and adjust for double input frequency at TP5.
50. Repeat steps 48 and 49 using a 100 kHz input. Adjusting only variable capacitor C147 for minimum signal at TP5.

Channel A

51. Set both VOLTS RMS ranges to .001-2 V rms by applying a +0.4 volts or logic 0 pins 23 and 24 of the BCD connector.
52. Remove inputs from generator, both channel A and B. Connect both positive and negative inputs of channel A and B to circuit ground.
53. Connect scope to TP1 and adjust R187 for zero volts of offset with scope on 5 mV/cm range. Change phase range between ±180° range and 0/360° range. Adjust R187 for minimum dc variation between ranges, this may be slightly different from 0 volts.
54. Remove inputs from circuit ground. Connect generator to both channel A and B inputs as shown in Figure 4-1[C]. Set generator for 10 kHz, 10 mV and adjust C11 for minimum signal at TP2. Increase input to 1 V rms and adjust C11 for minimum signal of frequency doubling.
55. Repeat step 54 using a 100 kHz input adjusting only variable capacitor C11 for minimum signal.

4.2.6.3 ATTENUATOR COMMON MODE REJECTION ADJUSTMENT

56. Set both VOLTS RMS ranges to .3-300 by applying +2.4 volts or logic 1 to pins 23 and 24 of BCD connector and apply a 7 V rms 250 Hz sine wave to both inputs as shown in Figure 4-1[C].
57. Connect scope probe to test point TP2, and circuit ground and adjust R200 for minimum signal.
58. Increase input frequency to 25 kHz, and adjust C5 for minimum amplitude at TP2.
59. Connect scope probe to test point TP5, decrease input frequency to 250 Hz, and adjust R199 for minimum signal.
60. Increase input frequency to 25 kHz, and adjust C68 for minimum amplitude at TP5.
61. Repeat steps 51 through 55 if needed.

4.2.7 Auto Range Calibration

With the volt meter connected between the wiper of R16 and ground, adjust R16 for 3.5 volts ±1%. Connect the volt meter between the wiper of R12 and ground and adjust R12 for 0.1 volts ±10 mV.

4.3 CORRECTIVE MAINTENANCE

If the Model 755 Phase Meter appears to be operating abnormally, and an investigation of input/output connections, as well as a calibration check, do not cure the problem; follow the trouble-shooting procedure outlined below.

Trouble	Check
1. Readout jumping around when no input signal is applied.	Normal operation, the high sensitivity of the input picks up external 60 Hz noise.
2. Readout scattering occasionally with low input amplitude and/or frequency.	Noise spikes are riding on input signal or signal-to-noise ratio is too high. Put 0.1 μF capacitors, or matched filters, across inputs.
3. Readout scattering randomly with input signal applied.	a. Check that phase angle is not within 2° of RANGE extreme. Use other RANGE setting. b. Reduce ground loops, and use differential inputs isolating grounds.
4. Erroneous phase reading.	a. Check both VOLTS RMS settings. Overdrive causes phase errors. b. Quick check CALIBRATE limits. c. If "a" and "b" do not help, apply same input to both channels, select −180°/+180° RANGE and, if reading is not 000.0, recalibrate Zero Crossing Board.
5. Display not lighted when POWER is set to ON.	Check fuse. Check +180 V, ±15 V, ±3.6 V, and +5 V power supplies
6. Two digits light in same lamp.	Defective display lamp.
7. Display locked on maximum or minimum full scale regardless of inputs.	a. If locked on maximum, Channel A Zero Crossing has no output. b. If locked on minimum, Channel B Zero Crossing has no output. c. If not "a" or "b" check IC4 on the Logic and Power Supply Board.
8. Input loading circuit being measured due to low input impedance.	Input FET Q1, Q2, Q14, or Q15 has been damaged. Replace with MPF104 or 2N5458 or equivalent.

If the instrument is not operating properly, and the above steps do not solve the problem, recalibrate the instrument as described in paragraph 4.2. If recalibration does not solve the problem, follow the procedure outlined below.

1. First check all power supplies for proper operation. If any are malfunctioning, refer to the Circuit Description as well as the schematic when trouble shooting the supply.
2. With 1 kHz 1 V rms sine wave applied to both inputs, look at Zero Crossing test points TP3 and TP6. If 1 V pulses at 1 kHz are not observed, read Circuit Description and refer to the schematic for trouble shooting.
3. If the proper pulses are seen in step 2 above, look at the junction of R65, R66, and R68. This point should show a square wave approximately 0 V to +3.6 V peak.
4. If the dc OUTPUT −10 mV/DEG is correct but the digital display is incorrect, recheck +180 V, +5 V, and ±3.6 V supplies. Refer to the timing diagram (Figure 3-6) and Circuit Description given in paragraph 3.2.3.

SECTION 5
DIAGRAMS ADDENDUMS AND PARTS LISTS

5.1 DIAGRAMS

The schematic diagrams within this manual are, wherever possible, arranged in the sequence followed in the circuit description. Whenever assembly drawings are included, they are positioned adjacent to the schematics for maximum information presentation and minimum page flipping. Additional voltage or waveform information, beyond that given in the circuit description, may be shown on the schematic diagrams, at test points and key locations throughout the instrument.

5.2 ADDENDUMS

Under WAVETEK's product improvement program, the latest electronic designs and circuits are incorporated into each WAVETEK instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made under a WAVETEK Engineering Change Notice (ECN) and these ECN pages are inserted immediately inside the rear cover. If no such pages exist, the manual should be correct as printed.

5.3 PARTS LISTS

Whenever possible, an assembly drawing and the associated parts list are kept to one piece of paper or are positioned for maximum information presentation. The following list of manufacturers should be used in conjunction with the parts lists. The abbreviations shown below are used in the "Manufacturer Key" column on the parts lists.

DRAWINGS

The following assembly drawings (with parts lists) and schematics will be included at the rear of this manual, in the arrangement shown below:

LEFT PAGE

CHASSIS ASSEMBLY
755-000 Sheet 1 of 2

LOGIC AND POWER SUPPLY ASSEMBLY
755-010

ZERO CROSSING BOARD ASSEMBLY
755-011

DIGITAL BOARD ASSEMBLY
750-012

MIN-MAX CALIBRATION
755-014

AUTO RANGE BOARD ASSEMBLY
755-015

ANALOG BOARD ASSEMBLY
270-011

REAR PANEL ASSEMBLY
755-000 Sheet 2 of 2

RIGHT PAGE

CHASSIS SCHEMATIC
755-200

LOGIC AND POWER SUPPLY SCHEMATIC
755-210

ZERO CROSSING BOARD SCHEMATIC
755-211

DIGITAL BOARD SCHEMATIC
750-212

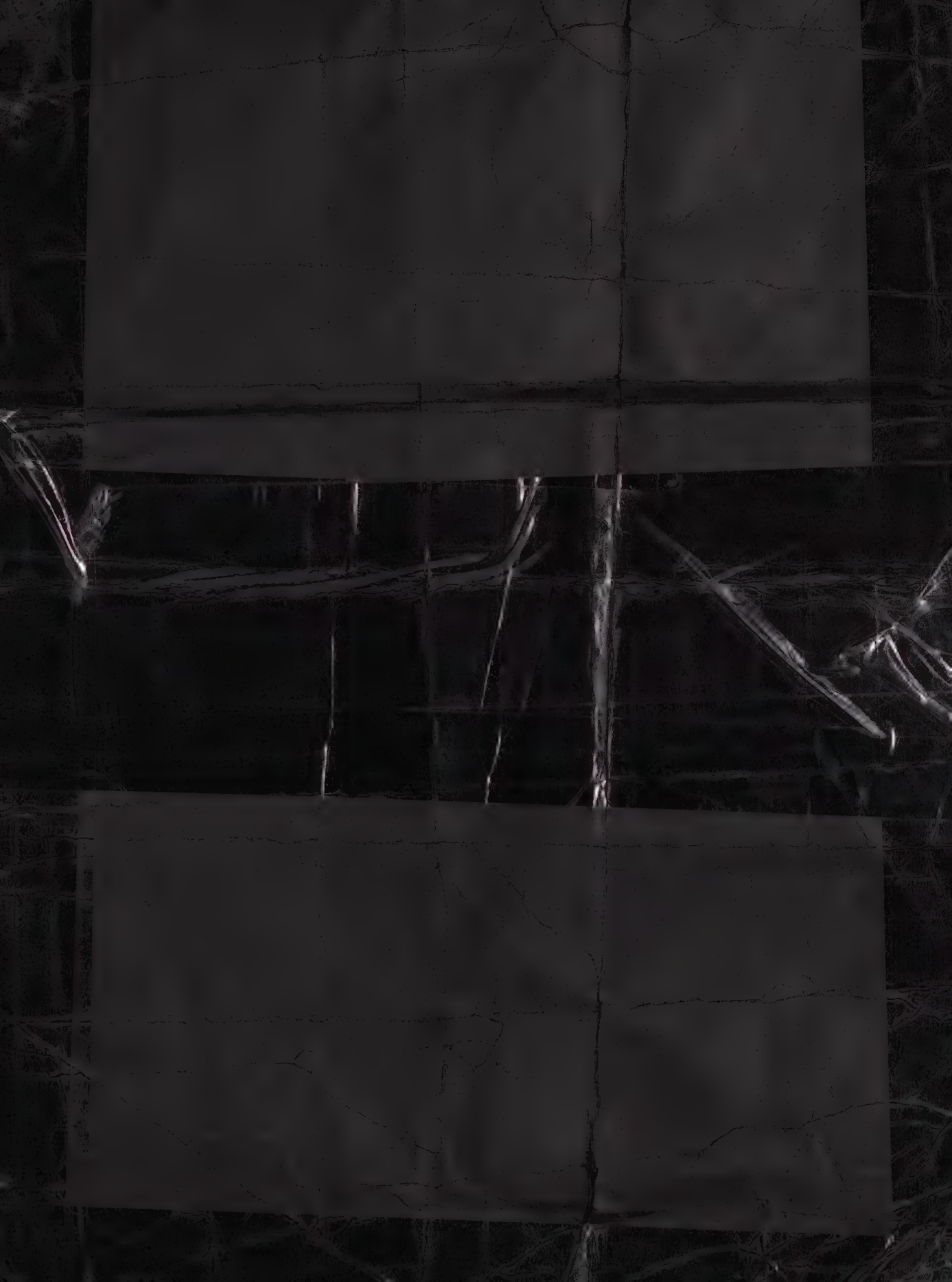
MIN-MAX CALIBRATION
755-214

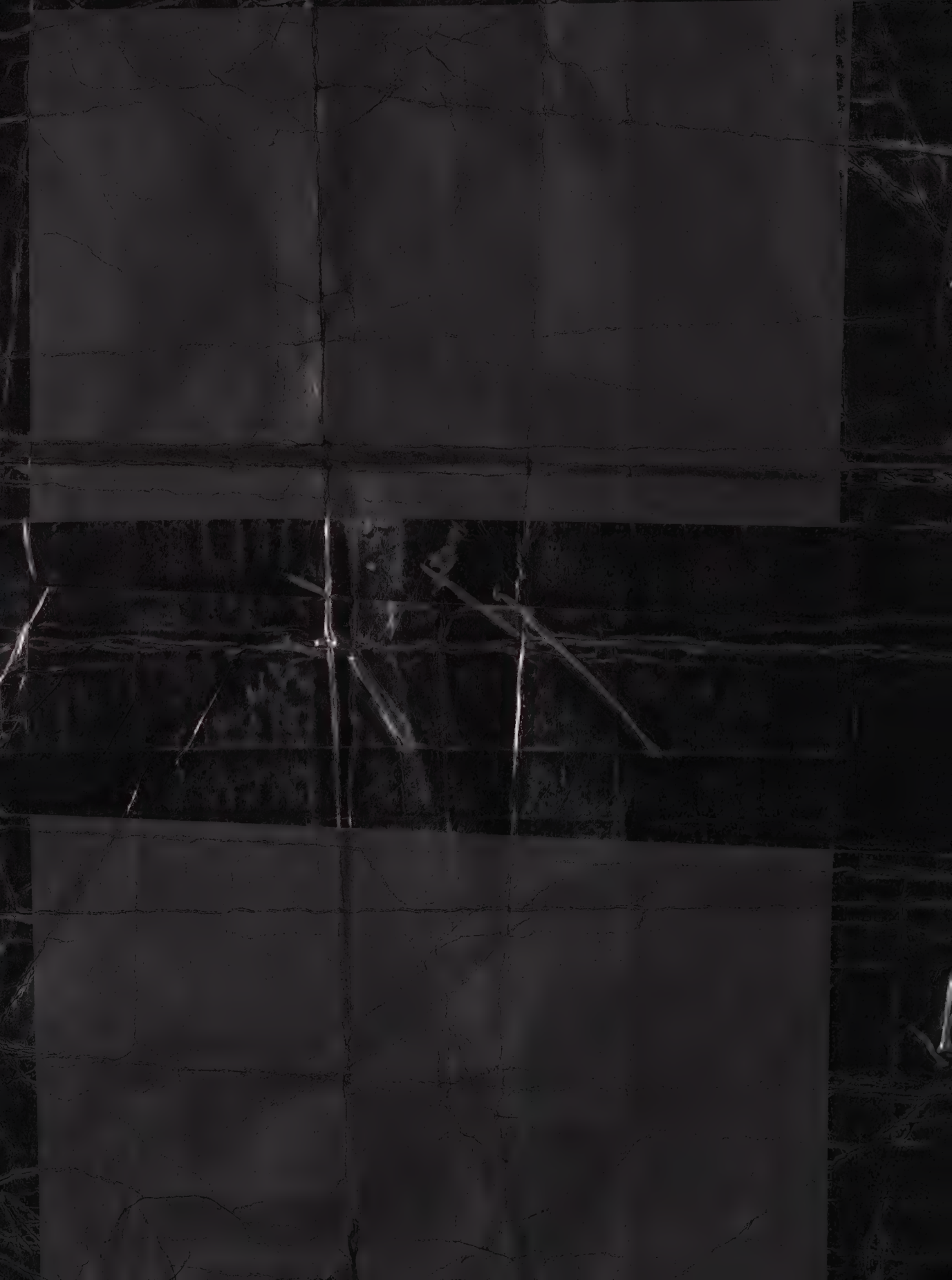
AUTO RANGE BOARD SCHEMATIC
755-215

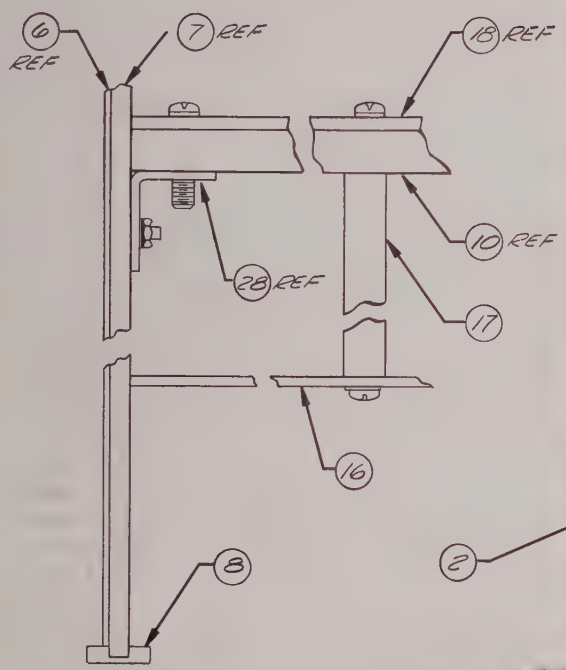
ANALOG BOARD SCHEMATIC
270-211

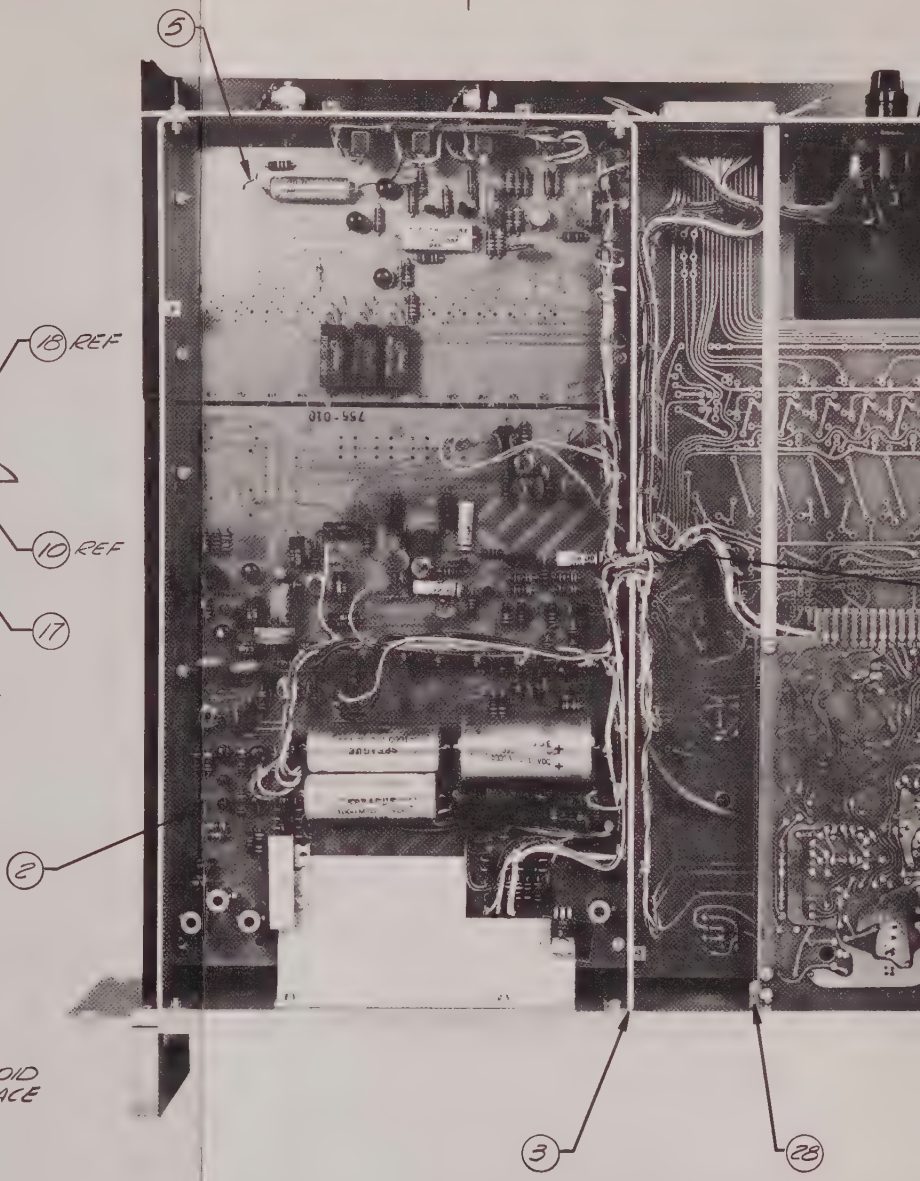
LIST OF MANUFACTURERS

A–B	Allen Bradley
A–E	Arco-Elmenco
AER	Aerovox
ALC	Alco Electronic Products Inc.
AMP	Amp Inc.
APL	Amphenol
APX	Amperex
A–R	American Radionics, Inc.
BEL	Belden
BMC	Budwig Mfg. Co.
BOU	Bourns
B–T	Boots-Townsend Aircraft
BUR	Burroughs
BUS	Bussman
CAM	Cambion
C–D	Cornell Dubilier
CGW	Corning Glass Works
C–J	Cinch Jones
C–K	C and K Components
C–L	Centralab
CTS	Chicago Telephone Systems
C–W	Continental Wire
DEU	Deutsch
DIO	Diodes Inc.
E–C	Electro Cube, Inc.
E–E	Elma Engineering
EFJ	E.F. Johnson Co.
ELC	Elco Corp.
ELP	Elpac Inc.
ETP	Erie Technoligical Products, Inc.
FCD	Fairchild
G–E	General Electric
G–H	Grayhill
G–R	General Radio Co.
HHS	Herman H. Smith, Inc.
H–P	Hewlett-Packard
IBM	IBM Industrial Products
IMB	IMB Electronics Products
IRC	International Resistance Company
JEF	Jeffers
KEI	Kings Electronics Inc.
LIT	Littelfuse
MAL	Mallory
M–C	Mura Corp.
MEK	Mektron
M–O	Marko-Oak
MOC	Micro-Ohm Corp.
MOL	Molex
MOT	Motorola
M–R	Milton Ross Co.
PPP	Phipps Precision Products
Q–C	Quality Components
QHM	Quality Hardware Mfg.
RCA	Radio Corporation of America
R–E	Richey Electronics
RMC	Radio Material Co.
ROS	Rosan Inc.
R–T	Rubber Teck Inc.
SCC	Stackpole Carbon Co.
SEL	Selectro
SEM	Semtech
S–I	Switchcraft Inc.
SLC	Shur-Lok Corp.
SPR	Sprague
S–T	Sarkes Tarzian
STR	Stettner & Co.
SUP	Superior Electric Co.
SYL	Sylvania
TAS	Teledyne Amelco Semiconductor Co.
T–I	Texas Instruments, Inc.
TRW	TRW Capacitor Division
USE	USECO Inc.
W–E	Wells Electronics
WEI	Wakefield Engineering Inc.



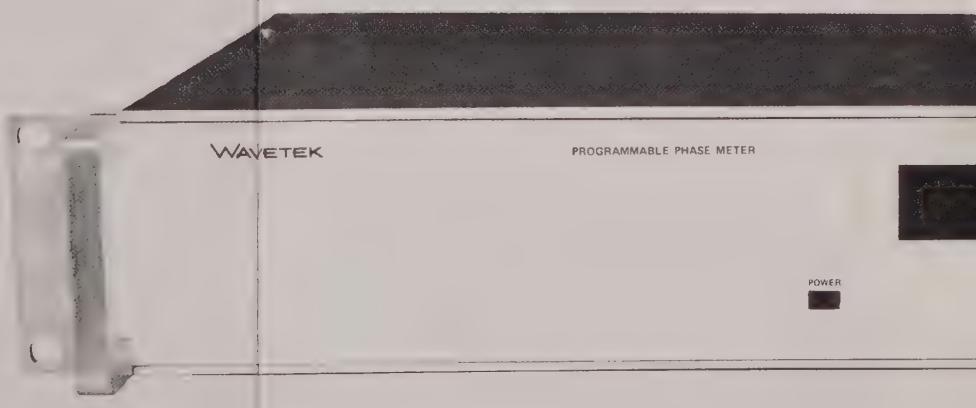


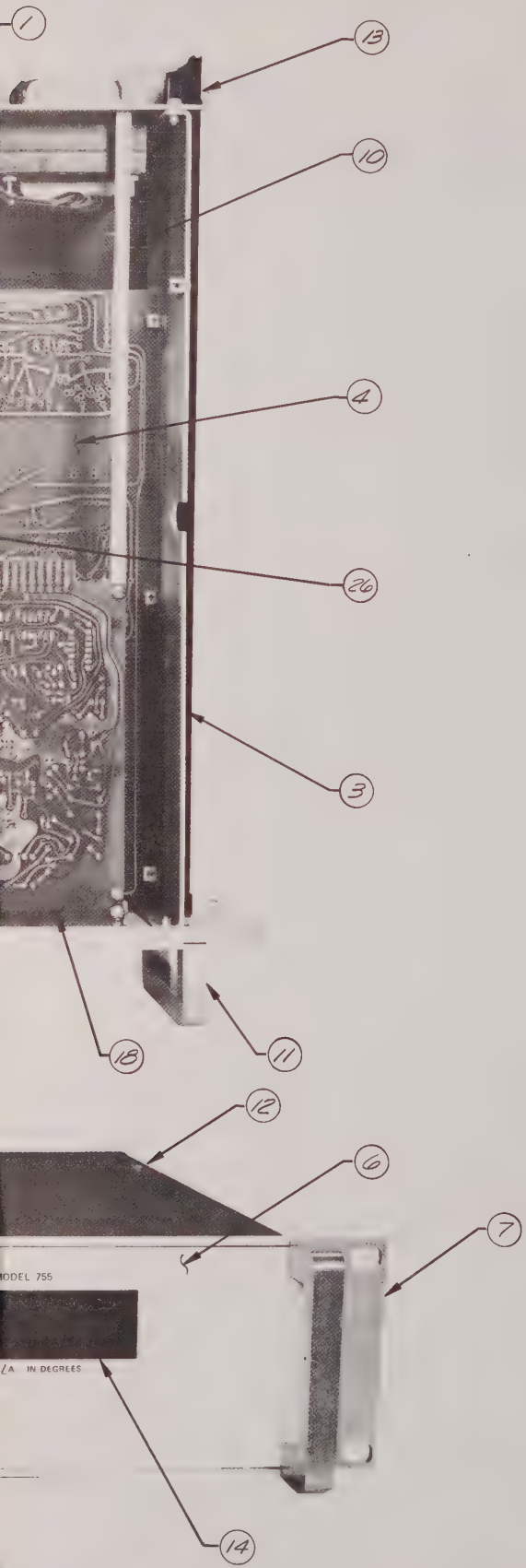




NOTE:
FRONT TRIM AND POLAROID MUST BE BONDED IN PLACE WITH SUITABLE AGENT.

NOTE:
1. ASTERISK (*) INDICATES ITEM NOT SHOWN



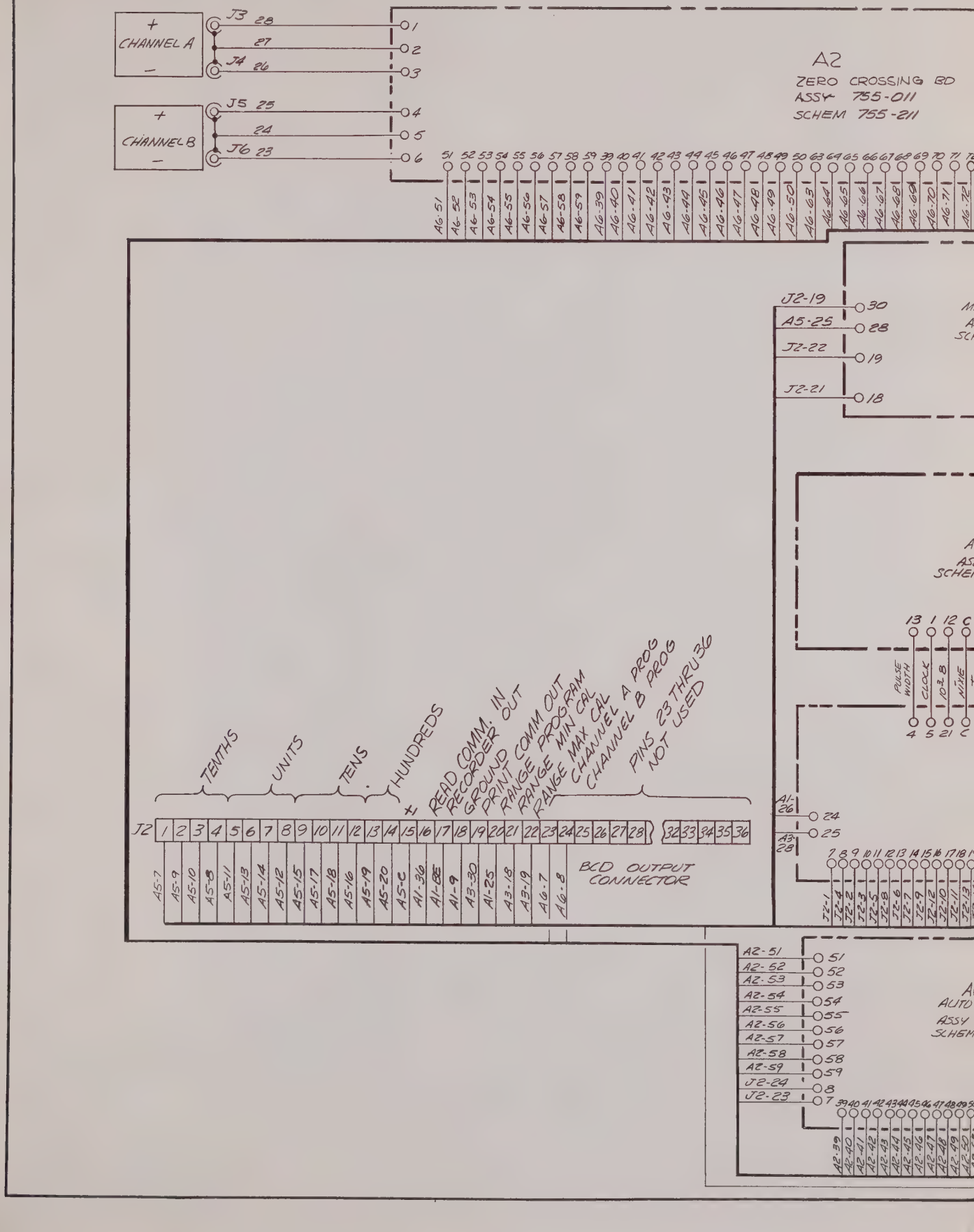


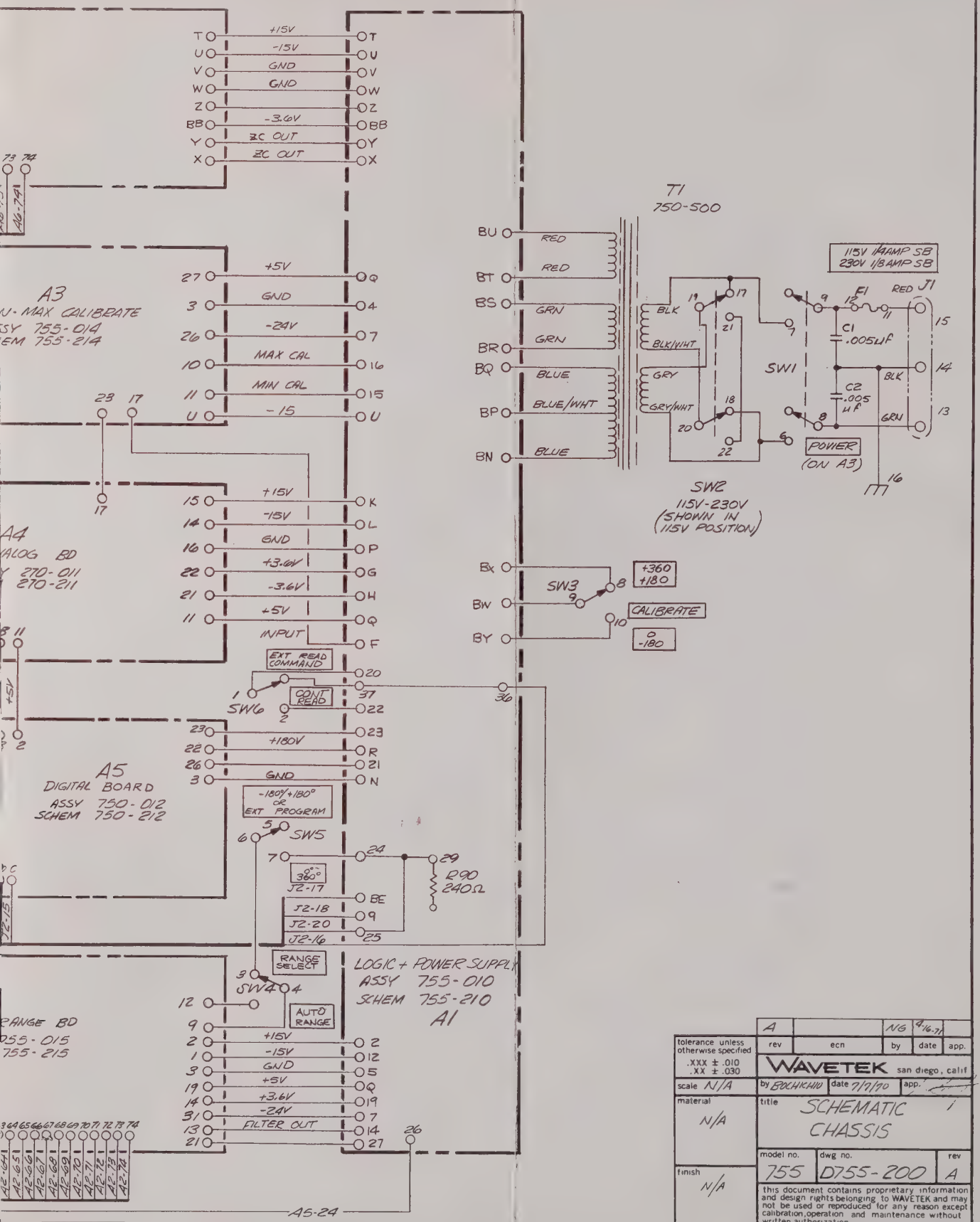
PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
1		REAR PANEL ASSY	WAVETEK	D755-000	1
2		POWER SUPPLY BD		D -010	1
3		SIDE & CENTER PLATE		C -001	3
4		MIN-MAX CALIB BD		D -014	1
5		AUTO RANGE BD		D -015	1
6		FRONT PANEL		C -312	1
7		SUB PANEL		C -313A	1
8		FRONT TRIM		B -307	2
9					
10		READOUT BAR		B -316	2
11		HANDLES		B -317	2
12		TOP COVER		C -318A	1
13		BOTTOM COVER		C -322A	1
14		READOUT WINDOW		A -323	1
* 15		ZERO CROSSING BD		D750-011	1
16		DIGITAL BOARD		D750-012	1
17		NIXIE STANDOFF		A750-313	4
18		ANALOG BOARD		D270-011	1
19					
20					
21					
* 22		POWER CORD	BELDEN	17258-S	1
23					
24					
25					
26		GROMMET	PLAS-TECH	MS-21266-1	A/R
27					
28		BRACKET	ELKAY	260	2
29					
30					

tolerance unless otherwise specified .XXX ± .010 .XX ± .030	rev	ecn	by	date / app
	WAVETEK san diego, calif			
scale N/A	by GRAY	date 8/21/70	app	
material N/A	title CHASSIS ASSY			
finish N/A	model no. 755	dwg no. SHT 1 OF 2 D755-000	rev	

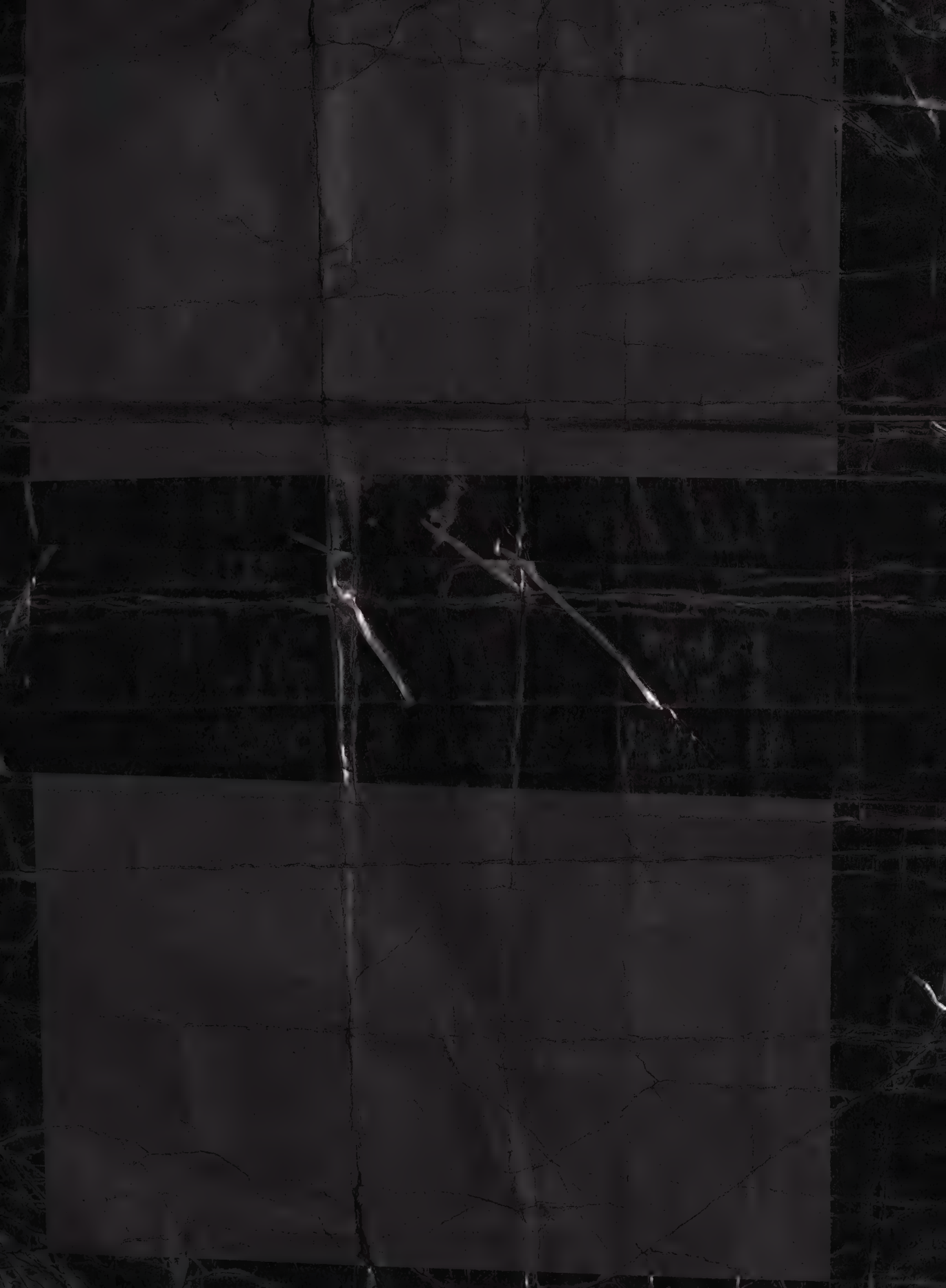
this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.

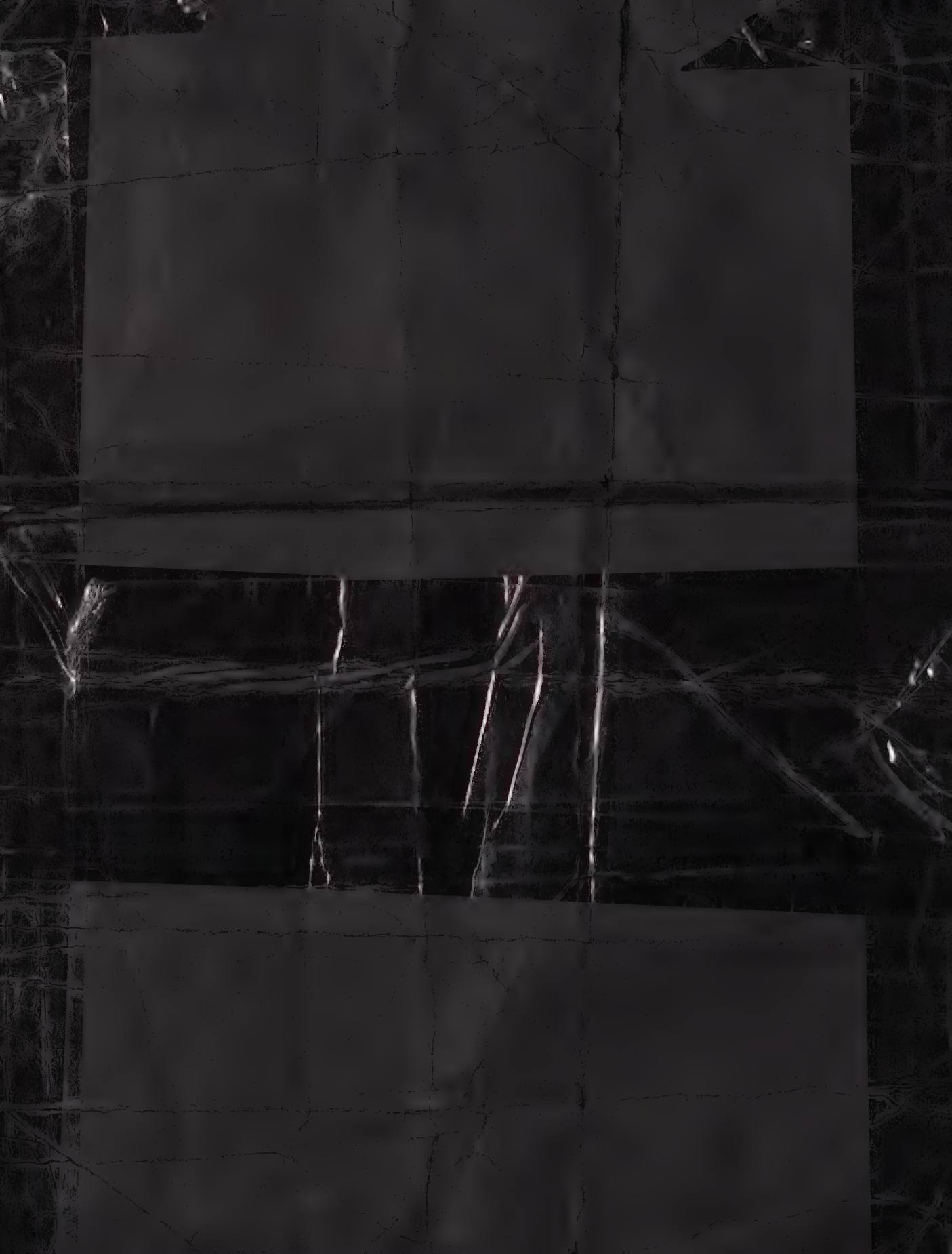

+
CHANNEL A
−
J3 28
27
J4 26
+
CHANNEL B
−
J5 25
24
J6 23
1
2
3
4
5
6
A2
ZERO CROSSING BD
ASSY 755-011
SCHEM 755-211
J2-19
A5-25
J2-22
J2-21
30
28
19
18
TENTHS
UNITS
TENS
HUNDREDS
±
READ COMM. IN
RECORDER OUT
GROUND
PRINT COMM OUT
RANGE PROGRAM
RANGE MIN CAL
RANGE MAX CAL
CHANNEL A PROG
CHANNEL B PROG
PINS 23 THRU 36
NOT USED
J2
BCD OUTPUT
CONNECTOR
PULSE WIDTH
CLOCK
10±8
MINE
A2-51
A2-52
A2-53
A2-54
A2-55
A2-56
A2-57
A2-58
A2-59
J2-24
J2-23
AUTO
ASSY
SCHEM

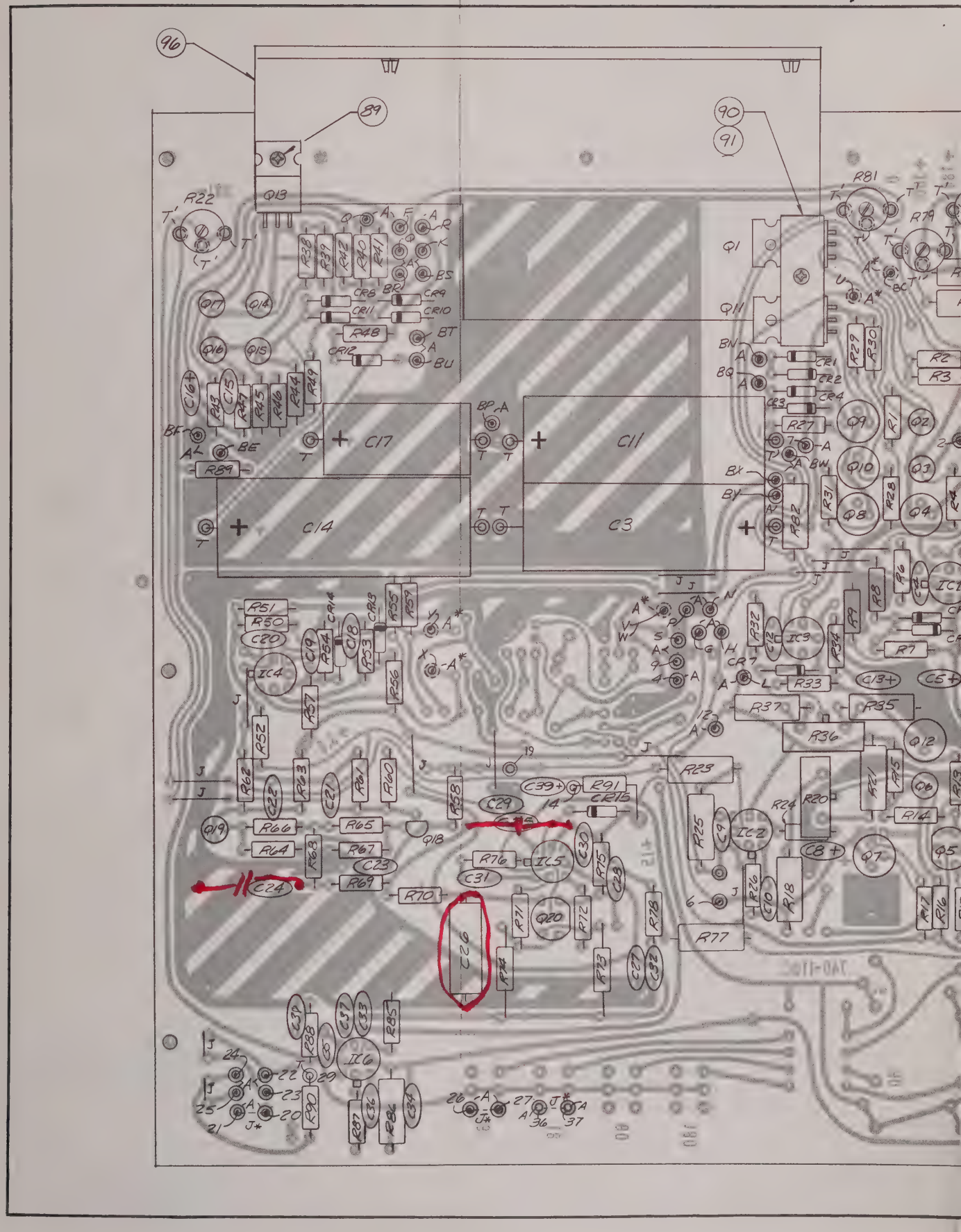


	A		NG	4-16-71	
tolerance unless otherwise specified .XXX ± .010 .XX ± .030	rev	ecn	by	date	app.
	WAVETEK san diego, calif				
scale N/A	by BOCHICHIO	date 7/9/70	app.		
material N/A	title SCHEMATIC CHASSIS				1
finish N/A	model no. 755	dwg no. D755-200			rev A

this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.






96
89
90
91
Q13
R22
Q1
Q11
R81
R79
C17
C11
C14
C3
IC4
IC3
IC2
IC5
IC6
Q20
Q18
Q19
C24
C22
R77
R23
R25
R24
R20
R18
R37
R35
R36
R33
C13+
C5+
C8+
R91
CR15
C39+
C29
C31
R76
R70
R58
R71
R72
R73
R74
R78
C27
C32
C30
C28
R75
R85
R88
R90
R87
R86
C34
C36
C37
C38
C33
C35
R64
R65
R66
R67
R68
R69
R63
R62
R61
R60
C21
C22
R57
R56
R55
R59
C18
C19
C14
CR8
CR9
CR10
CR11
CR12
R48
R49
R44
R45
R46
R47
R43
C15
C16+
R89
R51
R50
C20
R52
R53
R54
R38
R37
R42
R40
R41
Q17
Q14
Q16
Q15
R27
R30
R31
R28
R32
R34
R29
R26
R7
R8
R9
R12
R13
R14
R15
R16
R17
R19
C10
C9
C12
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q12
CR1
CR2
CR3
CR4
CR7
R82
R83
R84
R1
R2
R3
R4
R5
R6
BF
BE
BP
BQ
BN
BW
BX
BY
BT
BU
BS
BR
BC
J
J*
A*
T
T'
A
L
N
G
H
S
W
V
X
Y
Z
19
14
24
22
23
20
25
21
26
27
36
37
740-1190

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
1		CAPACITORS			
2	C9, C30, C35	CERAMIC DISC, 1000V, 10% 220PF	CRL	DD221	3
3	C18 C19 C21 C22	22PF		DD220	4
4	C6 C20 C23	20V 1% .1uf		UK20-104	3
5	C4, C10, C12 C15 C28 C31 C32 C34 C36 C38, C24	50V 10% .005uf		CK-502	11
6	C25	1000V, 10%, 560pf		DD 561	1
7	C17	ELECTROLYTIC 350V 4uf	SPRAGUE	TVA-1601	1
8	C5, C13	35V 27uf		196D276X0035C8	2
9	C8, C16, C39	15V 33uf		196D336X0015FB	3
10	C3 C11	35V 1000uf		39D108G035GLA	2
11	C14	15V 4000uf		39D408G015JL	1
12	C27 C29 C33 C37	CERAMIC DISC 50V, 10% .01uf	CRL	CK103	4
13					
14					
15					
16	CR1-CR4 CR8-CR11	DIODES	SEMTECH	SCE-1	8
17	CR5-CR7 CR15		FAIRCHILD	FD6666	4
18	CR12		SEMTECH	SCE-2	1
19	CR13, CR14		HP	HP 2811	2
20					
21					
22					
23		INTEGRATED CIRCUITS			
24	IC1-IC3 IC5 IC6	uA709	FAIRCHILD	uA709	5
25	IC4	CuL914		CuL914	1
26					
27					
28	Q1 Q13	TRANSISTOR TIP29	TI	TIP-29	2
29	Q11	TIP30		TIP-30	1
30	Q2 Q3 Q6 Q14-Q17	2N3565	FAIRCHILD	2N3565	7
31	Q4 Q8-Q10	2N3638		2N3638	4
32	Q12	(-39)		2N3638	1
33	Q18	2N3640		2N3640	1
34	Q7	2N3642		2N3642	1
35	Q19	2N3646		2N3640	1
36	Q5 Q20	TD101	SPRAGUE	TD101	2
37					
38					
39	R20	POTENTIOMETER 100Ω	CRL	BA1603-801	1
40	R36	1K		BA1603-803	1
41	R22, R79, R81	TYPE S - 500Ω (-41)	A/B	SV-5011	3
42	R84	1K (-45)		SV 1021	1
43					
44					
45	R71, R72	RESISTOR METALFILM, 1/4W, 1%, 1K	CORNING	RN60D	2
46	R16	2.37K			1
47	R34 R85	3.32K			2
48	R24	4.75K			1
49	R44	4.99K			1
50	R10 R14	5.76K			2
51	R7, R8, R38	10K			3
52	R15	19.1K			1
53	R68-R70	237K			3
54	R75	698K			1
55	R73, R74	2M			2
56					
57					
58		WIRE WOUND PRE-AGED			
59	R18	1% 2.37K	MICRO OHM	TYPE 143	1
60	R35	9.00K			1
61	R77	9.53K			1
62	R23	9.75K			1
63	R21, R25, R31 R80, R86	10K			5
64	R82 R83	19.6K			2
65					

PARTS LIST

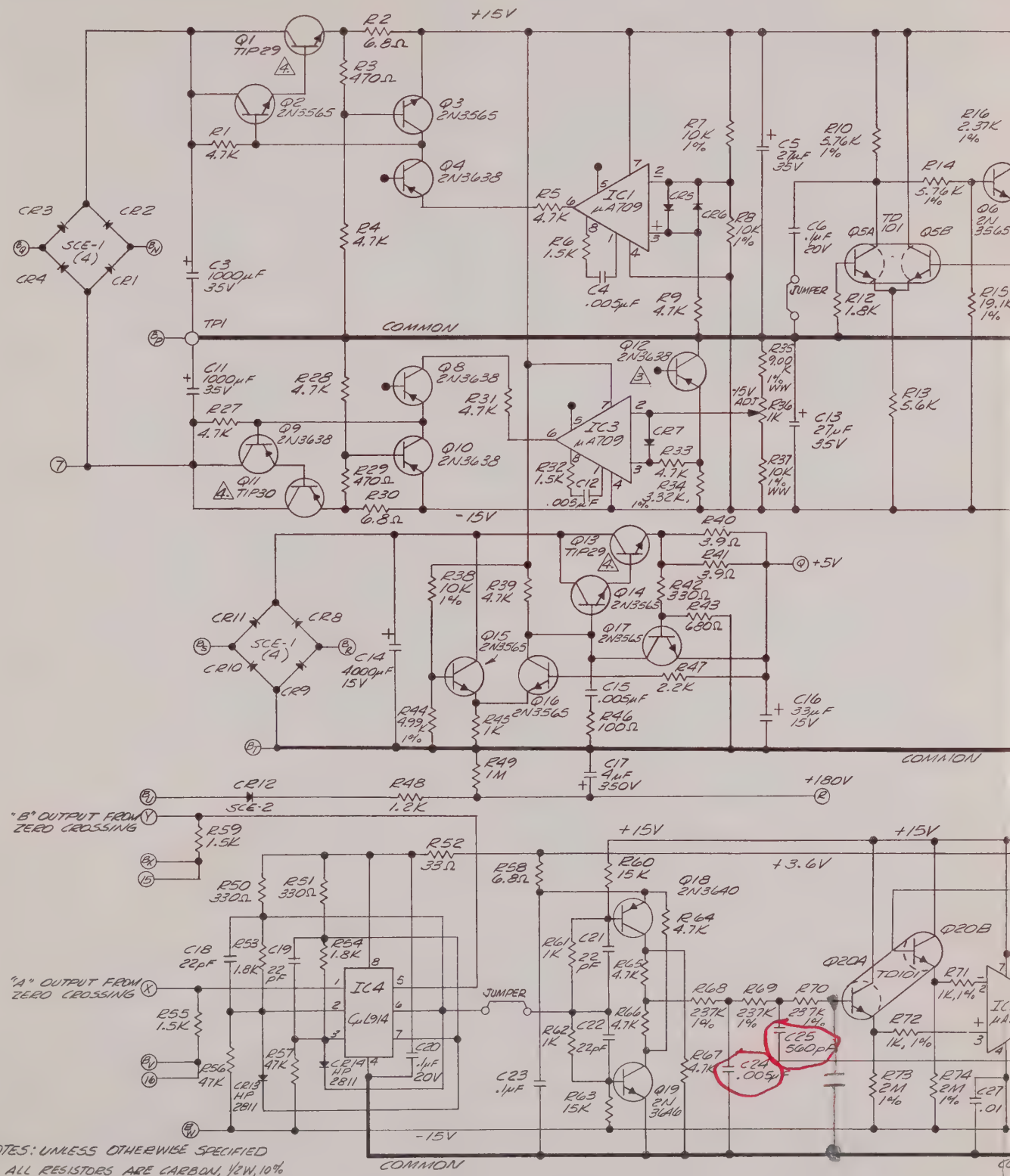
ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
66					
67	R40 R41	RESISTOR CARBON 1/2W 5% 3.9Ω	STACKPOLE	RC20GF3R9J	2
68	R2, R30, R58	6.8Ω		6R8J	3
69	R52	33Ω		330J	1
70	R46 R78, R88, R91	100Ω		101J	4
71	R7, R42 R50 R51	10% 330Ω		331K	4
72	R3 R29	470Ω		471K	2
73	R43	680Ω		681K	1
74	R45 R61 R62 R89	1K		102K	4
75	R48	1.2K		122K	1
76	R4, R26, R32 R55 R59 R76 R87	1.5K		152K	7
77	R12 R53, R54	1.8K		182K	3
78	R47	2.2K		222K	1
79	R1, R9, R5, R9 R27, R28, R31 R33 R39 R64-R67	4.7K		472K	13
80	R13	5.6K		562K	1
81	R60 R63	15K		153K	2
82	R56 R57	47K		473K	2
83	R49	1MΩ		105K	1
84	R90	240Ω		241K	1
85					
86					
87					
88					
89		NYLON SCREW	SMITH	2505	1
90		TRANSISTOR INSULATOR	WAVETEK	740-307A	2
91		HEATSINK	WAVETEK	130-311	2
92		TRANSIPADS	MILTON ROSS	10123N	6
93	A, A*	AMP PINS	AMP	61182-2	48
94	T	TERMINALS	USECO	2010B-1	9
95	T'	TERMINALS	USECO	2005B-1	12
96		HEATSINK	WAVETEK	755-320A	1
97		PRINTED CIRCUIT BOARD	WAVETEK	740-110C	1

NOTES UNLESS OTHERWISE SPECIFIED

1. A* INDICATE AMP PINS INSTALLED ON CIRCUIT SIDE
2. LETTERED AND NUMBERED DESIGNATIONS ARE FOR INTERWIRING PURPOSES SEE SCHEM 755-200
3. J* INDICATE JUMPER INSTALLED ON CIRCUIT SIDE

tolerance unless otherwise specified .XXX ± .010 .XX ± .030	rev	ecn	by	date	app.
	WAVETEK san diego, calif				
scale N/A	by BOCHICHIO	date 7-9-70	app		
material N/A	title ASSEMBLY LOGIC + POWER SUPPLY BD				
finish N/A	model no. 755	dwg no. D755-010	rev		

this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.



NOTES: UNLESS OTHERWISE SPECIFIED

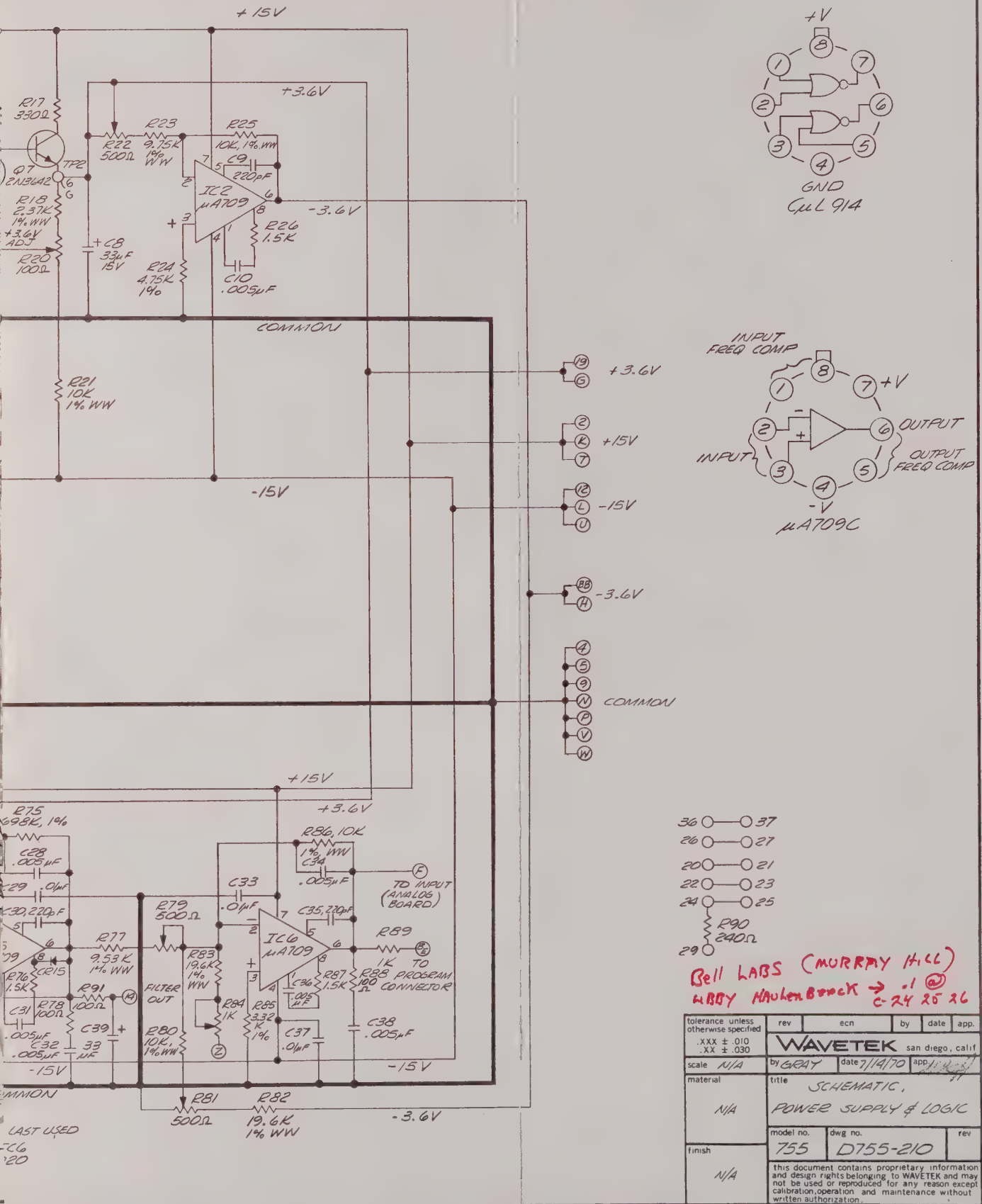
1. ALL RESISTORS ARE CARBON, 1/2W, 10%
2. ALL DIODES ARE FDG666

△3 SELECTED

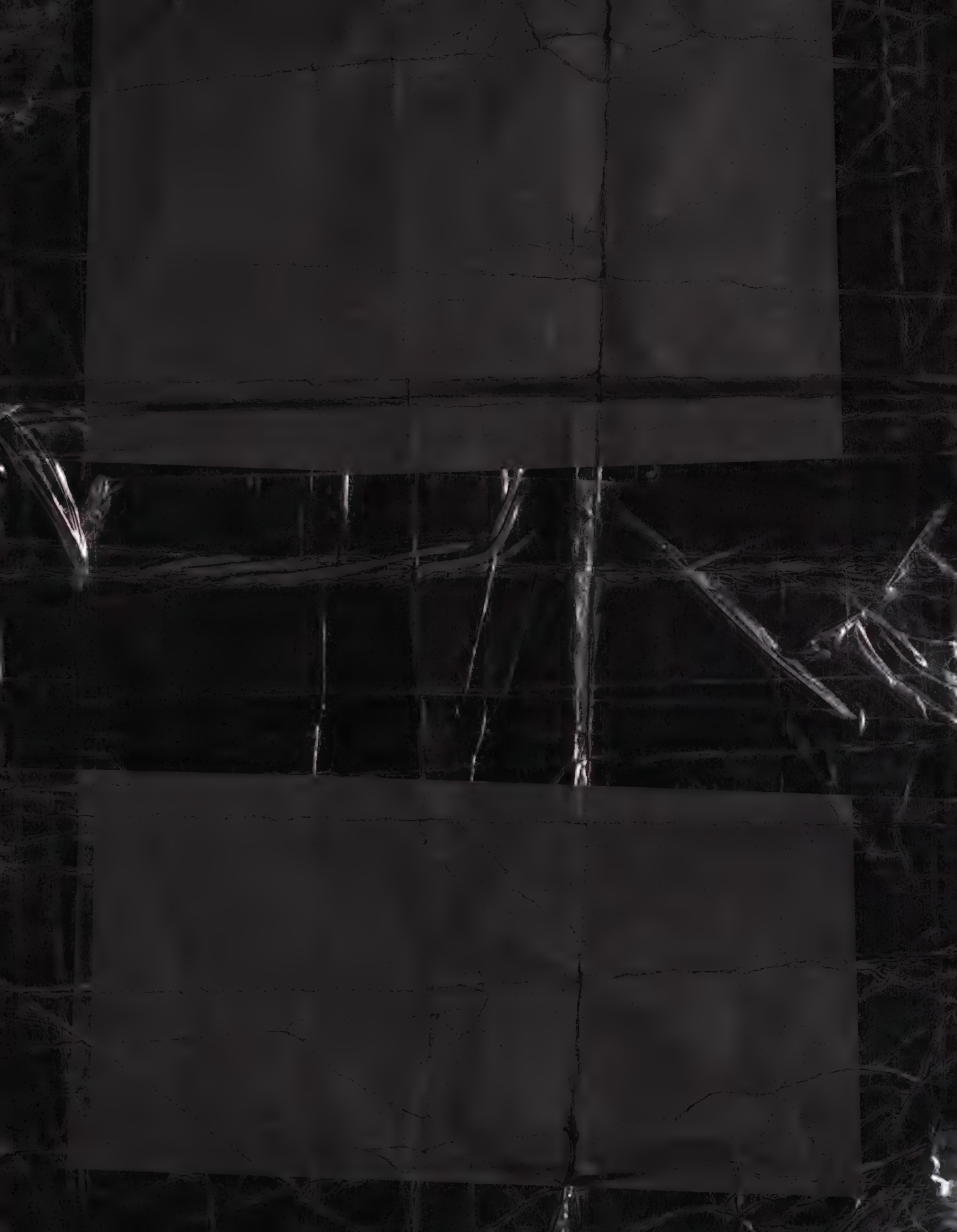
△4 COMPONENTS ARE MOUNTED ON REAR BRACKET ASSEMBLY

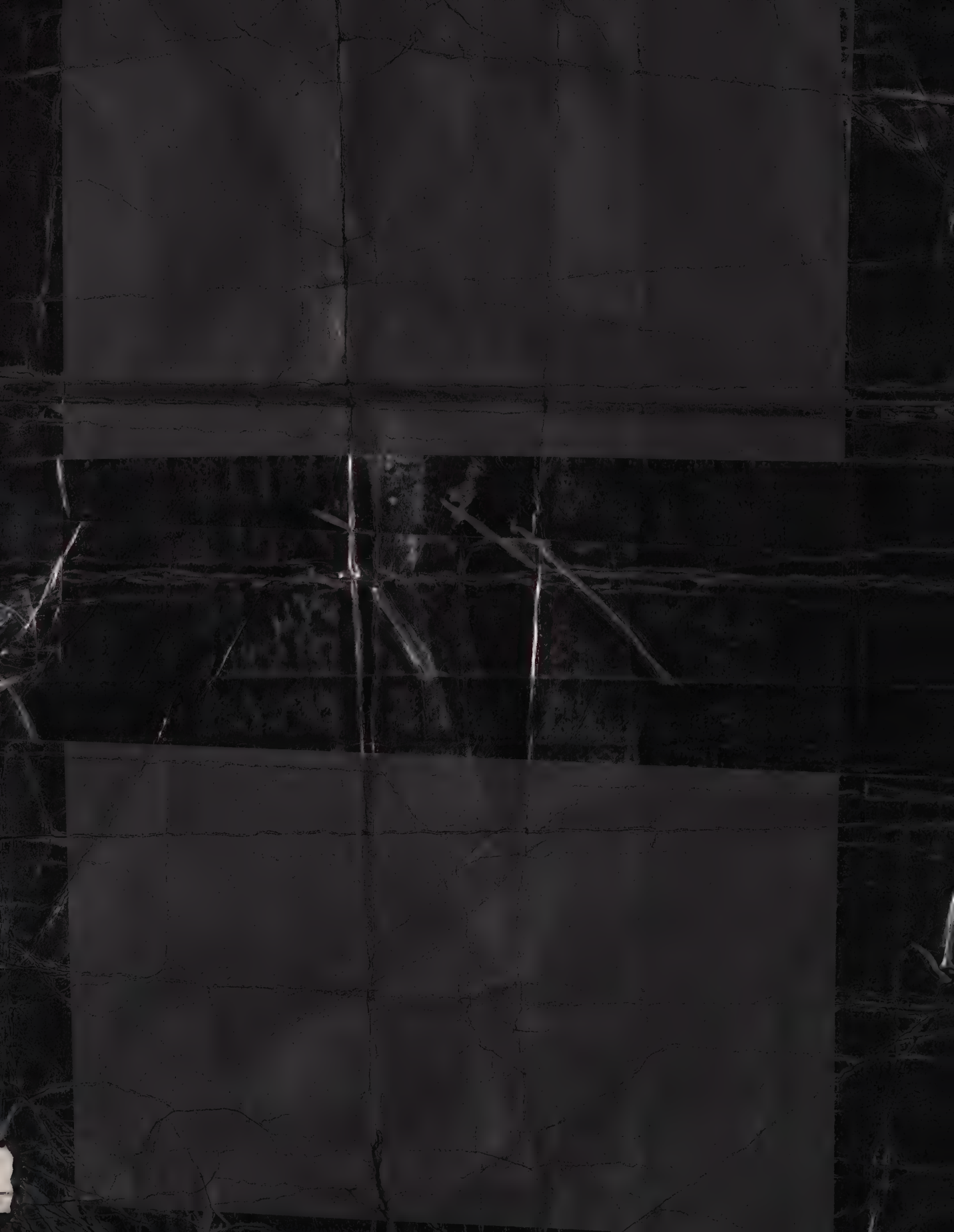
5. NUMBERED AND LETTERED TERMINATIONS INDICATE WIRING POINTS, SEE SCHEMATIC 755-200

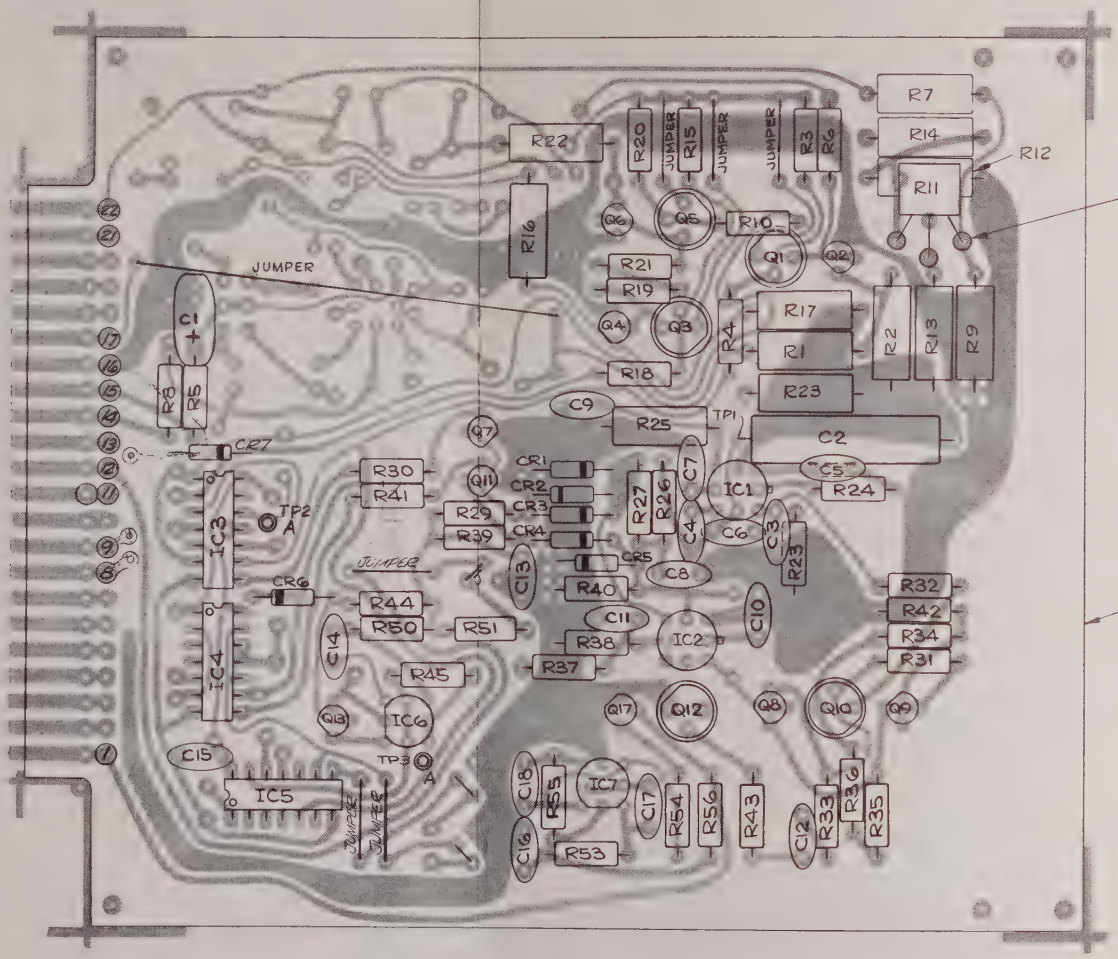
REF DES
C39
R91
CR15



tolerance unless otherwise specified .XXX ± .010 .XX ± .030	rev	ecn	by	date	app.
	WAVETEK san diego, calif				
scale N/A	by GRAY	date 7/14/70	app.		
material N/A	title SCHEMATIC, POWER SUPPLY & LOGIC				
	model no. 755	dwg no. D755-210			rev
finish N/A	this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.				







NOTES UNLESS OTHERWISE SPECIFIED:-

1. ALL JUMPERS ARE SLEEVED.
2.
3. FOR INTERCONNECTIONS REFER SCHEMATIC D750-200
4. A INDICATES AMP PIN MOUNTED FROM NEAR SIDE.
5. NO SUBSTITUTION SHALL BE ALLOWED FOR PART NOTED.
6. R53 & R55, MF ON STANDARD 755
7. LETTER DESIGNATIONS ARE INTERCONNECTION POINTS.

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFG BY	MFG No.	QTY
1					
2	C4	CAPACITOR, DISC, 22 pf 1KV	CRL	DD220	1
3	C14	47 pf 1KV		DD470	1
4	C12	470 pf 1KV		DD471	1
5	C17	.0015 μfd 1KV		DD152	1
6	C18	.0022 μfd 1KV		DD222	1
7	C5, C6, C8,	.005 μfd 50V		CK502	3
8	C3, C7, C9, C10, C11, C13, C15, C16	.01 μfd 50V		CK103	8
9	C2	MYLAR 1 μfd 1% 200V	ELECTROCUBE	210-B1C-105F	1
10	C1	TANTALUM 27 μfd 35V	SPRAGUE	196D276X0035FB	1
11					
12					
13					
14					
15					
16	IC3, IC4	MC863P INTEGRATED CIRCUIT	MOTOROLA	MC863P	2
17	IC5	MC856P		MC856P	1
18	IC6, IC7	CμL914	FAIRCHILD	CμL914	2
19	IC1	μA709 (-44)		μA709	1
20	IC2	μA710		μA710	1
21					
22					
23					
24					
25					
26	CR1 THRU CR7	FD6666 DIODE	FAIRCHILD	FD6666	7
27					
28					
29					
30	Q1, Q3, Q5 Q10	2N3638 TRANSISTOR	FAIRCHILD	2N3638	4
31	Q7, Q8, Q9, Q11 Q13, Q17	2N3646		2N3646	6
32					
33	Q2, Q4, Q6	2N4250 (5)	FAIRCHILD	2N4250	3
34	Q12	2N3638 (-46)	FAIRCHILD	2N3638	1
35					
36					
37					
38					
39		CIRCUIT BOARD	WAVETEK	270-111C	1
40		AMP PIN	AMP	61182-2	2
41		TERMINAL	USECO	2005B-1	3
42		TRANSIPAD	MILTON ROY	10123N	5
43					

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFG BY	MFG No.	QTY
44	R5, R8	22 Ω 1/2 WATT CARBON 10%	STACKPOLE	RC206F-220K	2
45	R32	82 Ω		-820K	1
46	R28	100 Ω		-101K	1
47	R33	220 Ω		-221K	1
48	R37, R38	560 Ω		-561K	2
49	R3, R15, R20, R36 R42, R43, R45, R54, R56	1K		-102K	9
50	R4, R10, R18, R26, R27, R30, R31, R44 R44, R50, R51,	2.2K		-222K	11
51	R40	4.7K		-472K	1
52	R6, R19, R21	8.2K		-822K	3
53	R29, R35, R39	10K		-103K	3
54	R34	62K 5%		-623J	1
55					
56	R24	1.5K 10%		-152K	1
57					
58					
59					
60	R9, R12	49.9Ω WIREWOUND (-43) 1%	MICRO OHM		2
61	R25	10K (-43)			1
62	R2, R7, R13, R14 R16, R17, R22, R23	30.1K (-43)			8
63	R1	137K (-43)			1
64					
65					
66					
67					
68	R53, R55	21.5K METAL FILM 1/4 WATT 1%	CORNING	RNG0D	2
69	NOTE 6	12.1K			
70					
71					
72	R11	1K POTENTIOMETER TYPES (-45)	AB	3V1021	1
73					
74					
75					

rev	ecn	by	date	app
C	ECN 317	NG	10/29/70	
B	ECN 306	NG	7/15/70	
A	ECN-294	BL	12/1/70	

tolerance unless otherwise specified
.XXX ± .010
.XX ± .030

WAVETEK san diego, calif

scale 2X | by L. ADAMSON | date 8/1/69 | app

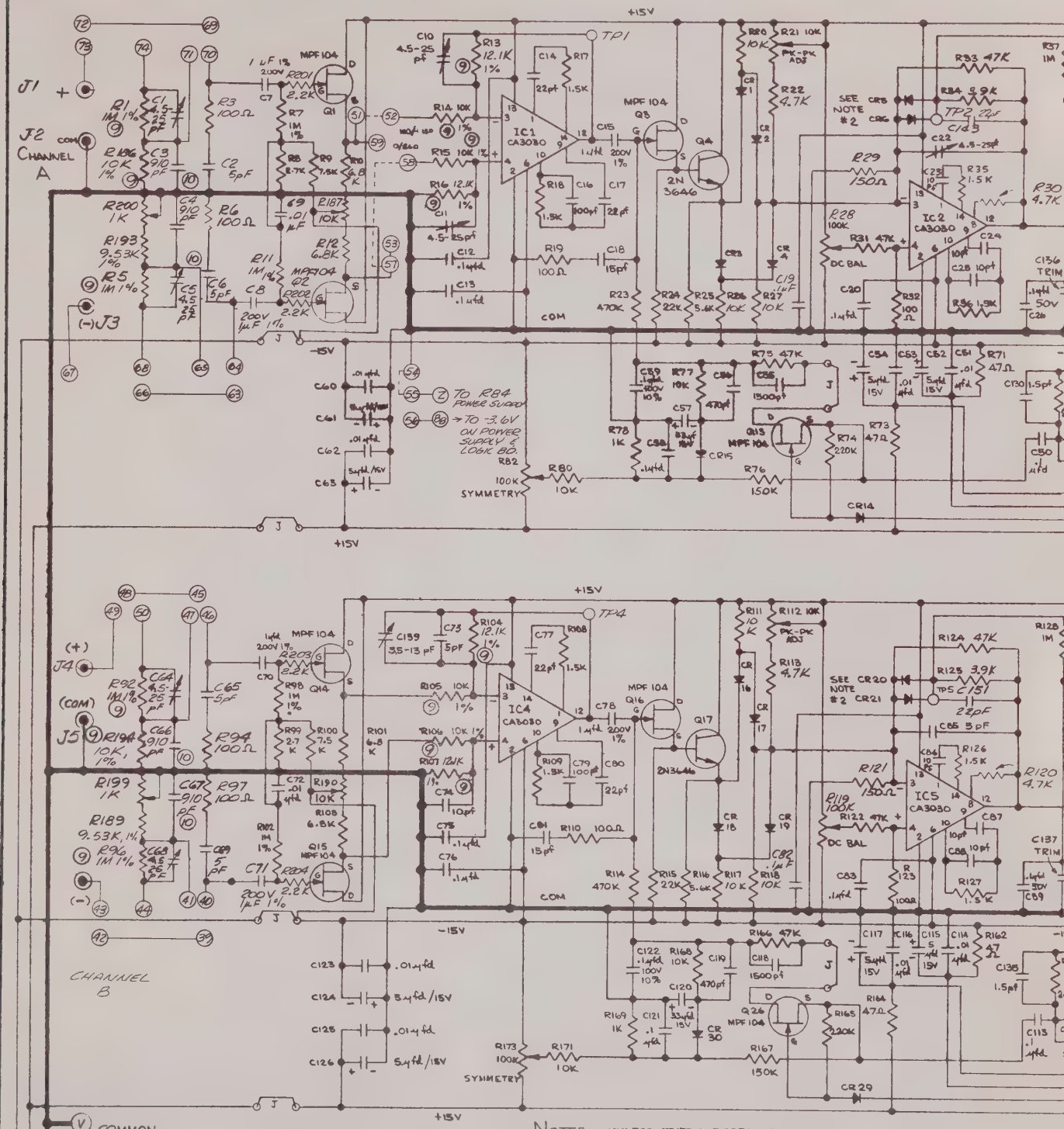
material

finish N/A

title
ASSEMBLY,
ANALOG BOARD

model no. 270,750 & 755 | dwg no. D270-011 | rev C

this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.

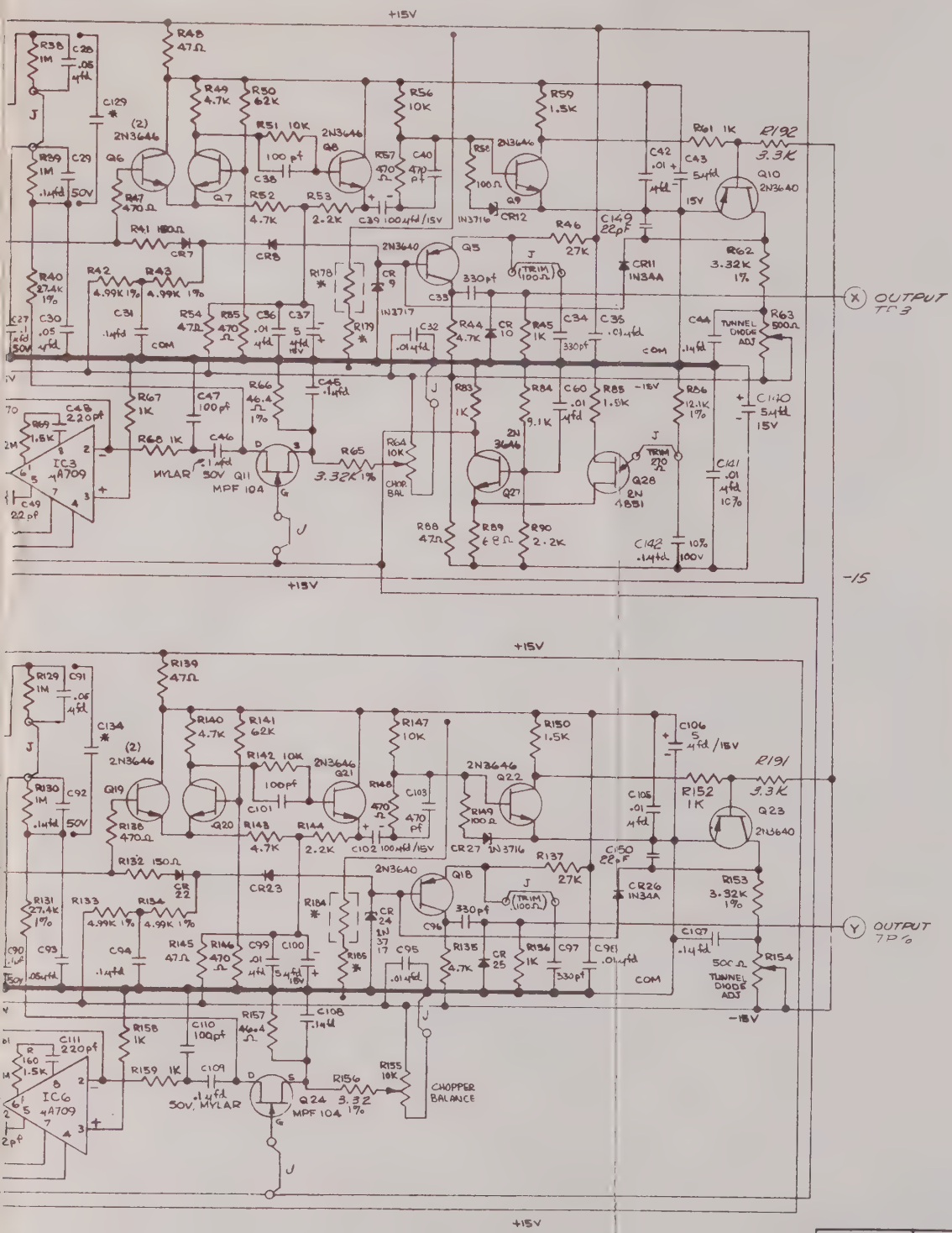


LAST COMP DES. USED

CR30 C131
R209 Q28
TP6 IC6

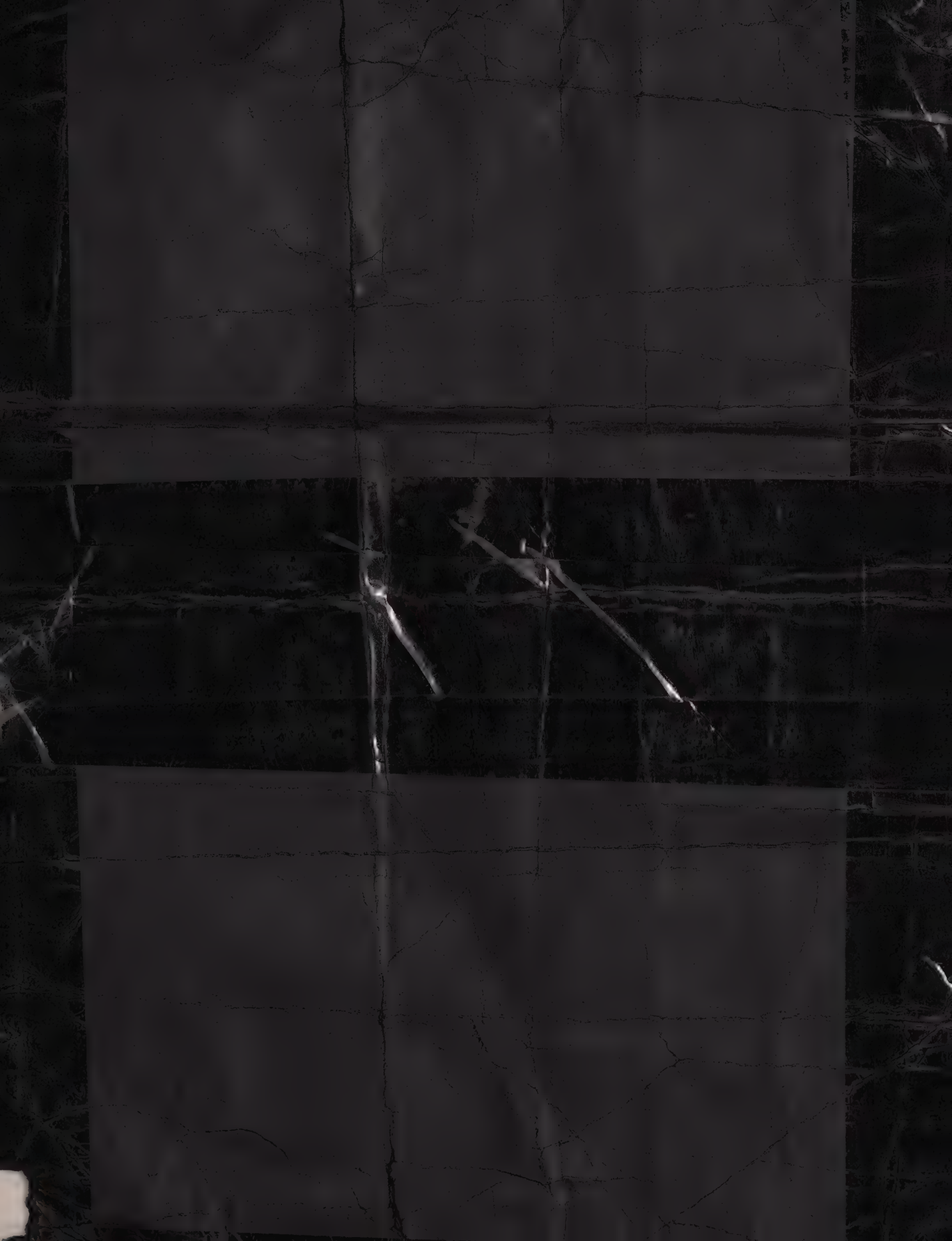
NOTES:- UNLESS OTHERWISE SPECIFIED -

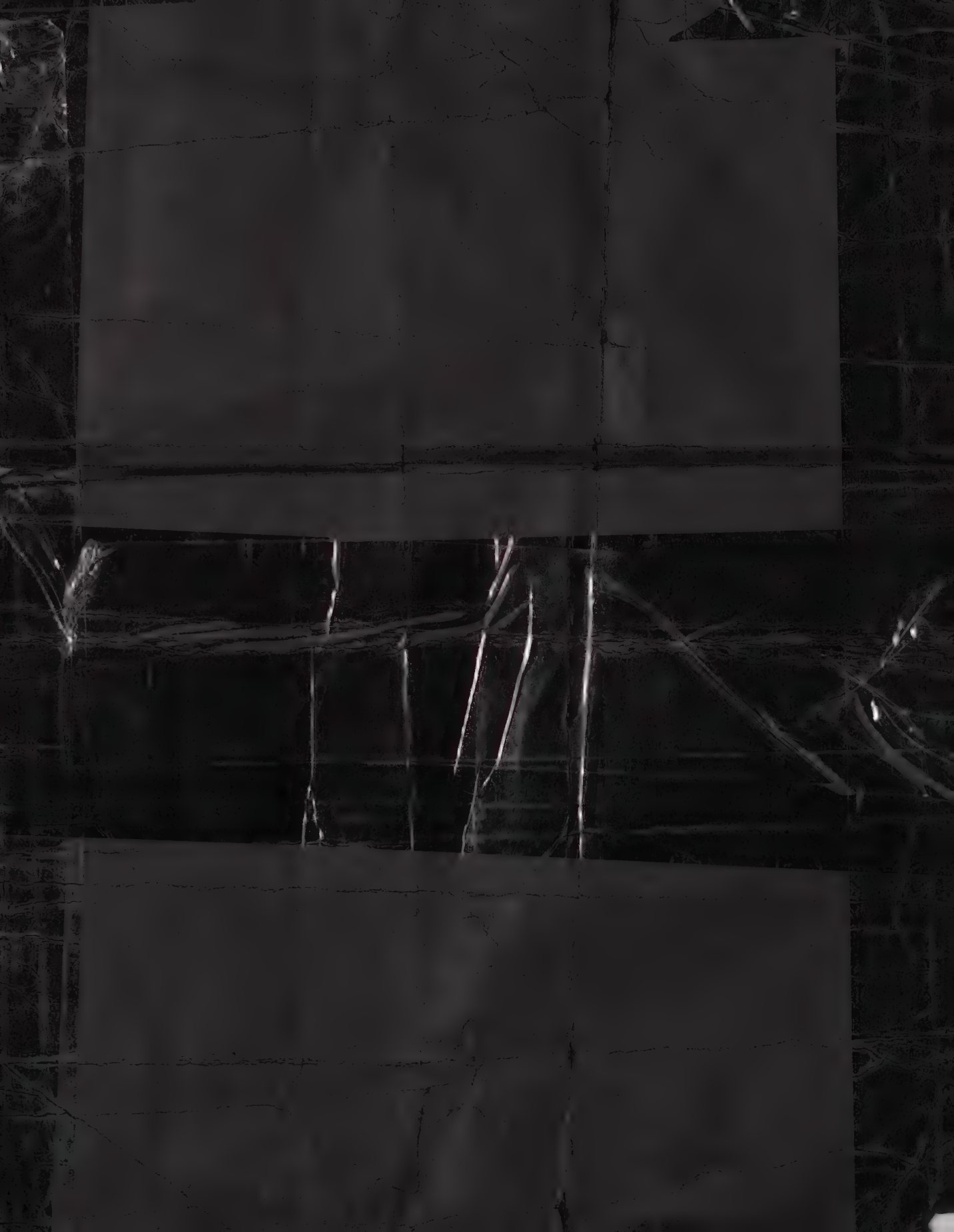
1. ALL RESISTORS ½ WATT, 10% CARBON
2. HP 2811 DIODES MATCHED
3. ALL DIODES FD6666
4. * INDICATES PROVISIONAL COMPONENTS (R174 THRU R185, R72 & R163 & C127, C128, C129, C132, C133 & C134)
5. R175, 176, 177, 181, 182 & 183 ARE 3.9Ω
6. C127, 128, 132, & 133 ARE 100 μfd
7. J INDICATES JUMPER
8. R72 & R163 ARE 1.5K
9. RN60D MATCHED SET
10. MATCHED SILVER MICA SET
11. LETTER DESIGNATIONS ARE INTERCONNECTION POINTS.

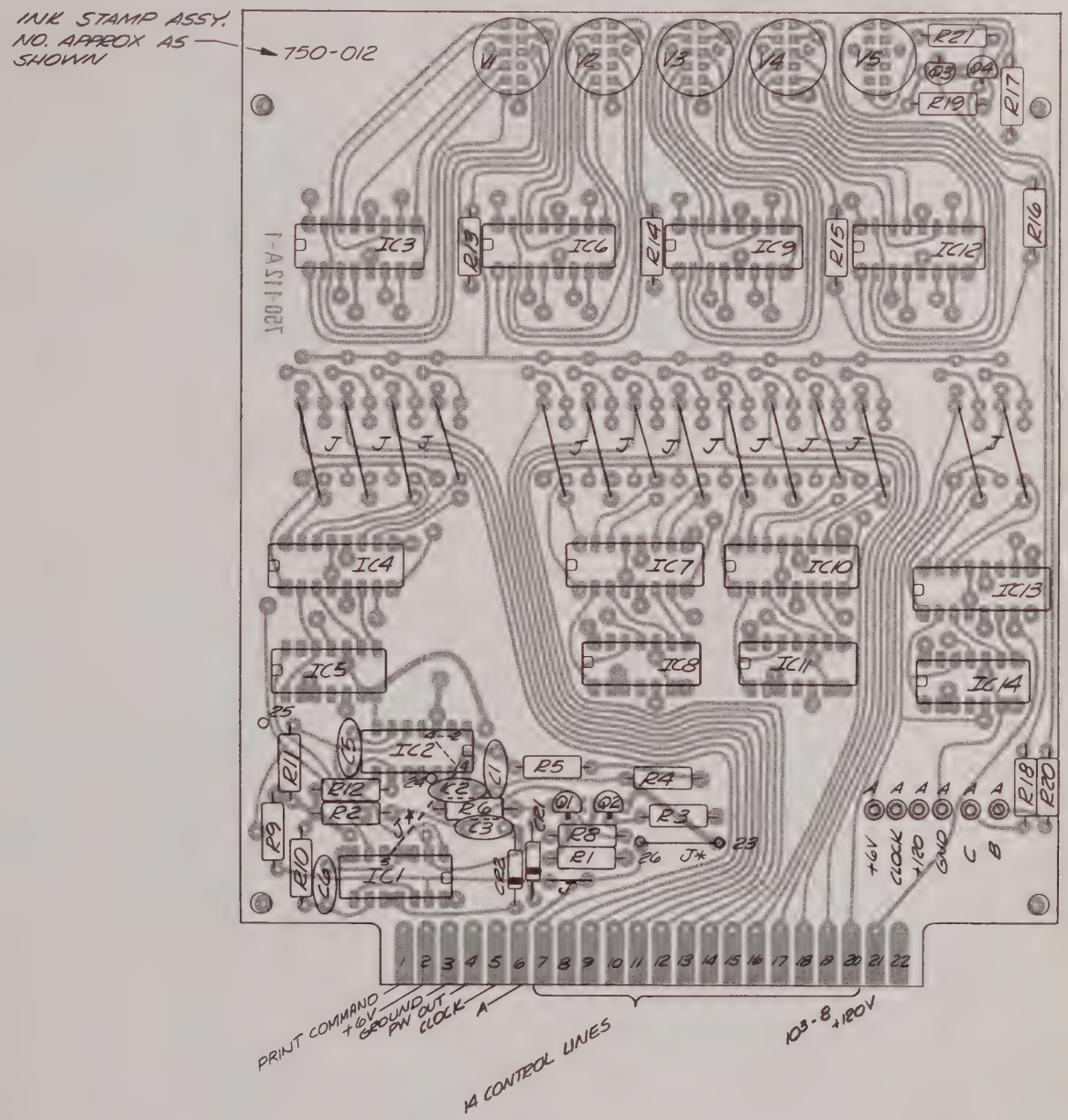


tolerance unless otherwise specified XXX ± 010 XX ± 030	rev	ecn	by	date	spp
	WAVETEK san diego, calif				
scale N/A	by GRAY	date 10/12/70	approved		
material N/A	title SCHEMATIC, ZERO CROSSING BOARD				
finish N/A	model no. 755	dwg no D755-211	rev		

this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.







NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPS MUST HAVE STRAIGHT LEADS
2. J* INDICATES MOUNTED ON CIRCUIT SIDE
3. J* INDICATES MODEL 750 ONLY

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO.	QTY
1		CAPACITORS			
2	C1, C2, C3, C6	CERAMIC DISC, 1 KV, 10%, .001μF	CRL	DD102	4
3					
4	C5	10V 0.47μF	SPRAGUE	HY-325	1
5					
6					
7					
8					
9		DIODES			
10	CR1, CR2	FD6666	FAIRCHILD	FD6666	2
11					
12					
13					
14		INTEGRATED CIRCUITS			
15	IC1, IC2	QUAD 2 INPUT NAND	MOTOROLA	SN7400	2
16	IC3, IC6, IC9, IC12	DECODER DRIVER		7441	4
17	IC4, IC7, IC10, IC13	QUAD LATCH		7475	4
18	IC5, IC8, IC11, IC14	DECADE COUNTER		7490	4
19					
20					
21					
22	V1-V4	NIXIE TUBES 0-9	BURROUGHS	B5750	4
23	V5	+, -		B5856	1
24					
25		RESISTORS			
26	R1, R3, R11, R12	CARBON, 1/2W, 10% 2.2K	STACKPOLE	RC20GF222K	4
27	R5	4.7K		472K	1
28	R18, R20	10K		103K	2
29	R13-R17	18K		183K	5
30	R9, R10	47K		473K	2
31	R2, R4, R6, R8	5% 750Ω		751J	4
32	R19, R21	10% 1M		105K	2
33					
34					
35					
36					
37	Q1, Q2	TRANSISTORS 2N3646	MOTOROLA	2N3646	2
38	Q3, Q4	MPS L01		MPS L01	2
39					
40					
41					
42					
43	◎A	AMP PINS	AMP	61182-2	6
44					
45					
46					
47					
48		DIGITAL BOARD	WAVETEK	750-112A	1
49					
50					

rev	ecn	by	date	app.
D	ECN 313	NG	1/8/70	
C	ECN 325	NG	1/26/70	
B	ECN 316	NG	1/14/70	

tolerance unless otherwise specified
.XXX ± .010
.XX ± .030

scale N/A

material N/A

finish N/A

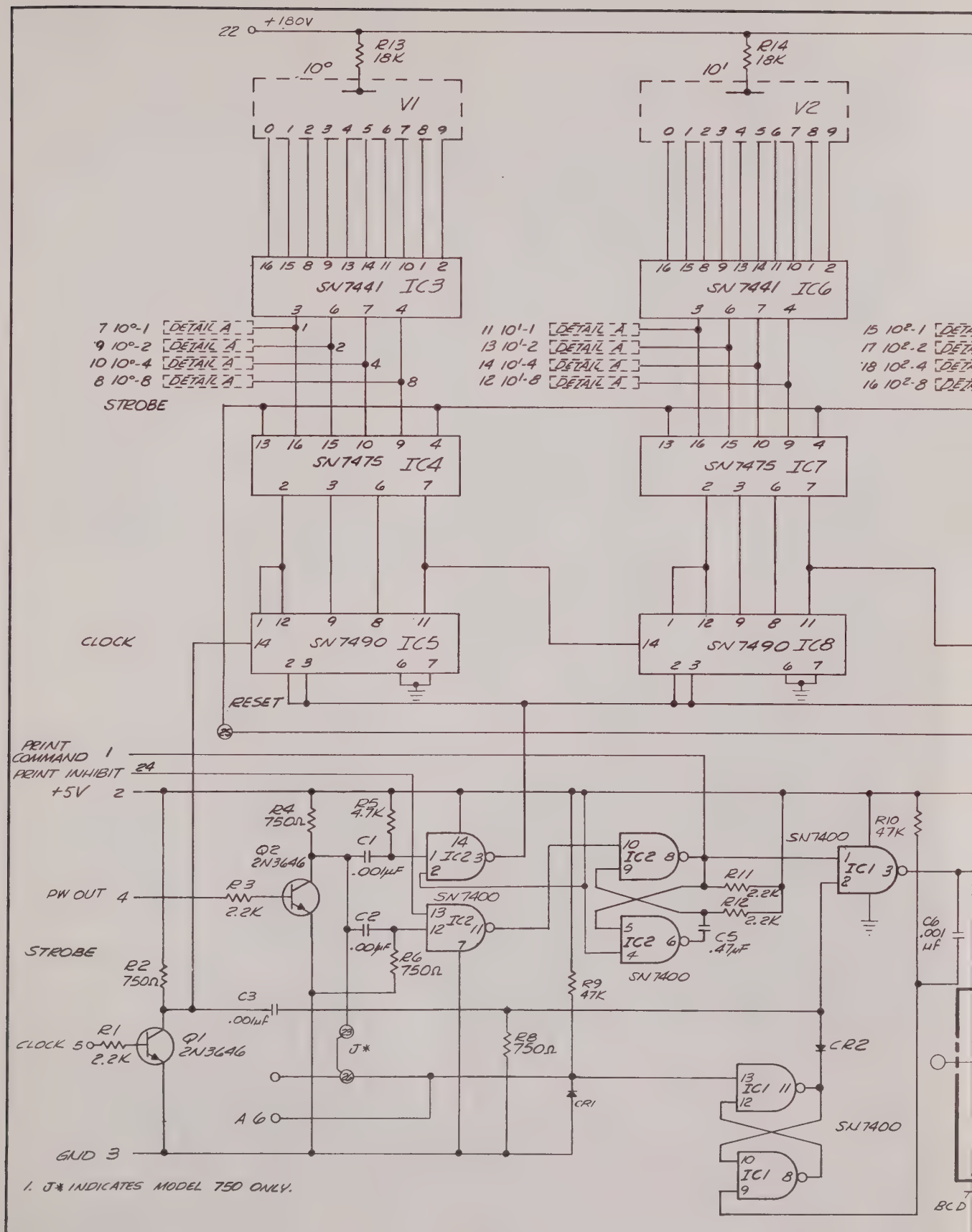
WAVETEK san diego, calif

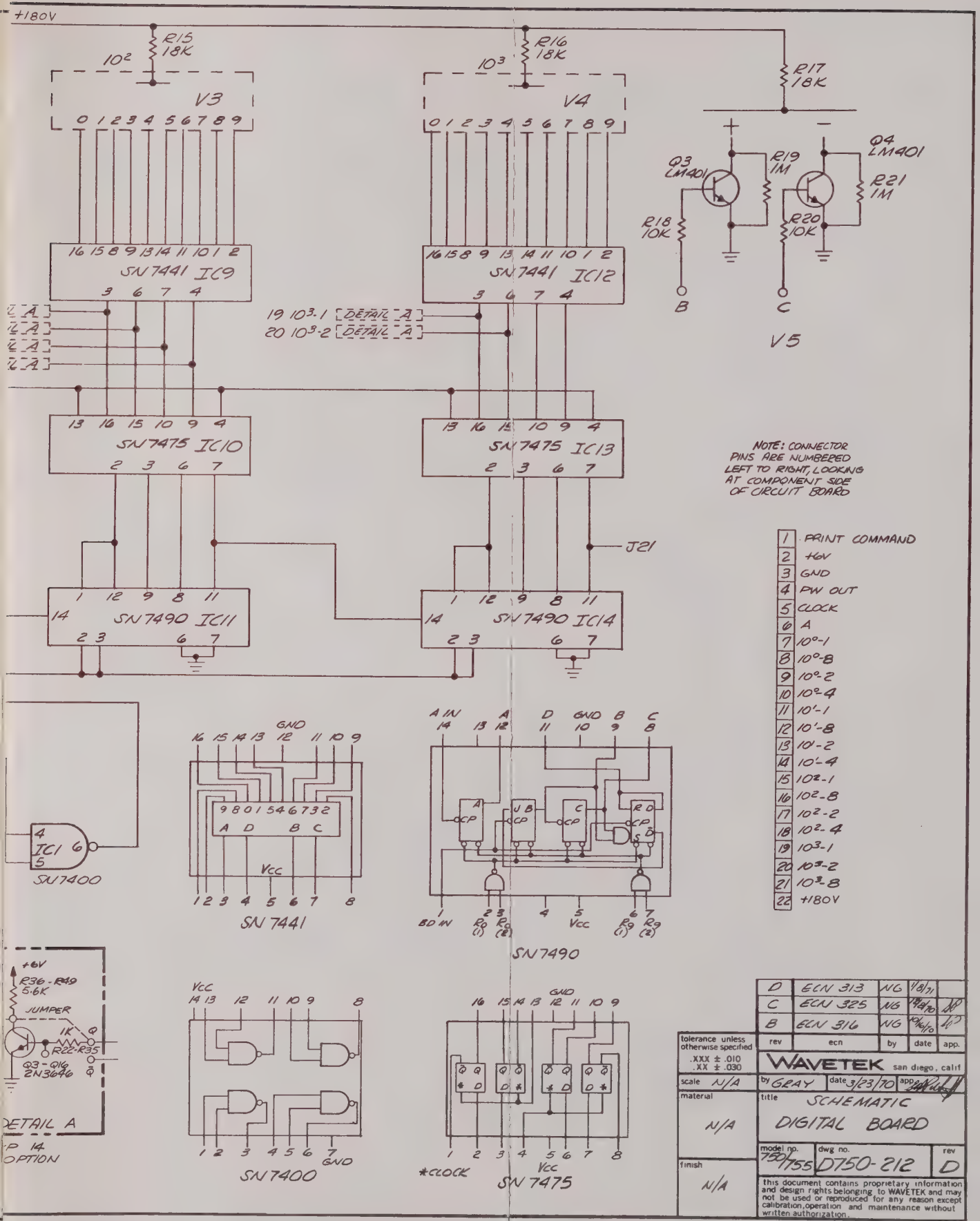
by BOCHICHIO date 4-20-70 app.

title
ASSY
DIGITAL BOARD

model no.	dwg no.	rev
750/755	D750-012	D

this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.


22 +180V
R13 18K
10°
V1
R14 18K
10'
V2
0 1 2 3 4 5 6 7 8 9
16 15 8 9 13 14 11 10 1 2
SN7441 IC3
SN7441 IC6
3 6 7 4
7 10°-1 DETAIL A
9 10°-2 DETAIL A
10 10°-4 DETAIL A
8 10°-8 DETAIL A
11 10'-1 DETAIL A
13 10'-2 DETAIL A
14 10'-4 DETAIL A
12 10'-8 DETAIL A
15 10²-1
17 10²-2
18 10²-4
16 10²-8
STROBE
13 16 15 10 9 4
SN7475 IC4
SN7475 IC7
2 3 6 7
1 12 9 8 11
14
SN7490 IC5
SN7490 IC8
2 3 6 7
CLOCK
RESET
PRINT COMMAND 1
PRINT INHIBIT 24
+5V 2
R4 750Ω
R5 4.7K
C1 .001μF
Q2 2N3646
PW OUT 4
R3 2.2K
C2 .001μF
R6 750Ω
STROBE
R2 750Ω
C3 .001μF
R1 2.2K
CLOCK 5
Q1 2N3646
J*
A 6
GND 3
R8 750Ω
R9 47K
CR1
CR2
IC2 3
IC2 8
IC2 11
IC2 6
SN7400
R11 2.2K
R12 2.2K
C5 .47μF
R10 47K
IC1 3
IC1 11
IC1 8
C6 .001 μF
BCD
1. J* INDICATES MODEL 750 ONLY.



rev	ecn	by	date	app.
D	ECN 313	NG	1/8/71	
C	ECN 325	NG	9/8/70	
B	ECN 316	NG	10/1/70	

tolerance unless otherwise specified .XXX ± .010 .XX ± .030

WAVETEK san diego, calif

scale N/A | by GRAY | date 3/23/70 | app.

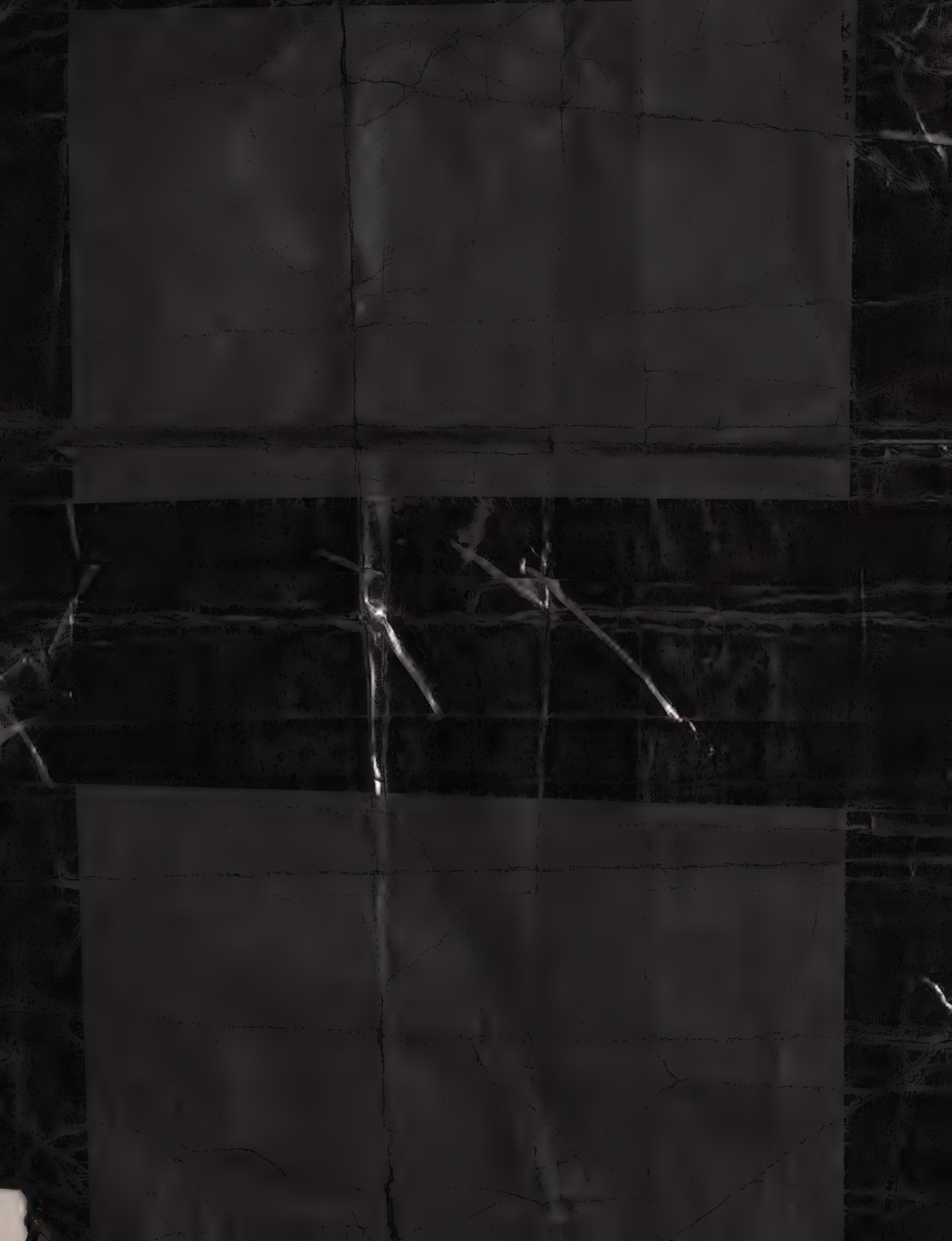
material N/A

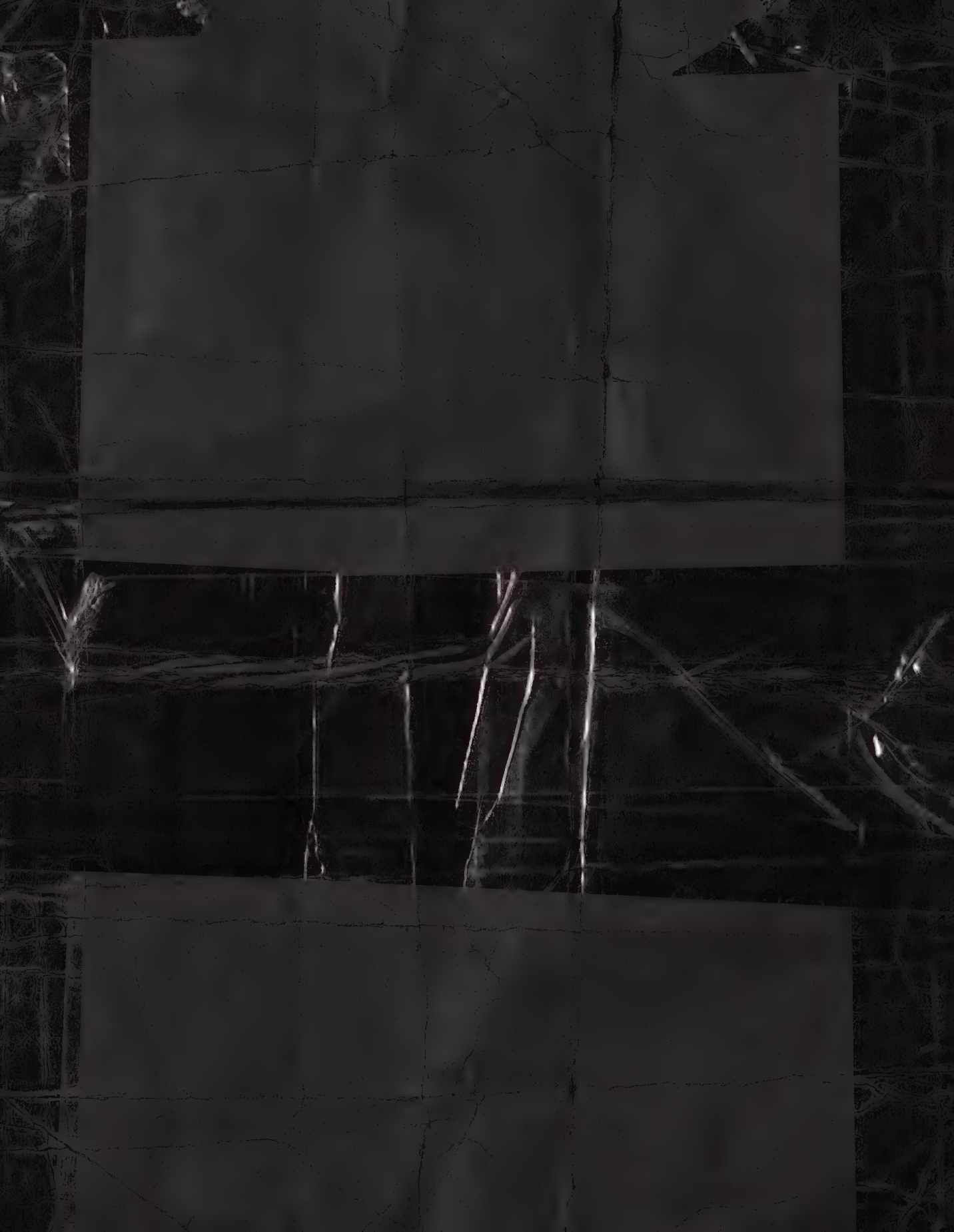
title SCHEMATIC DIGITAL BOARD

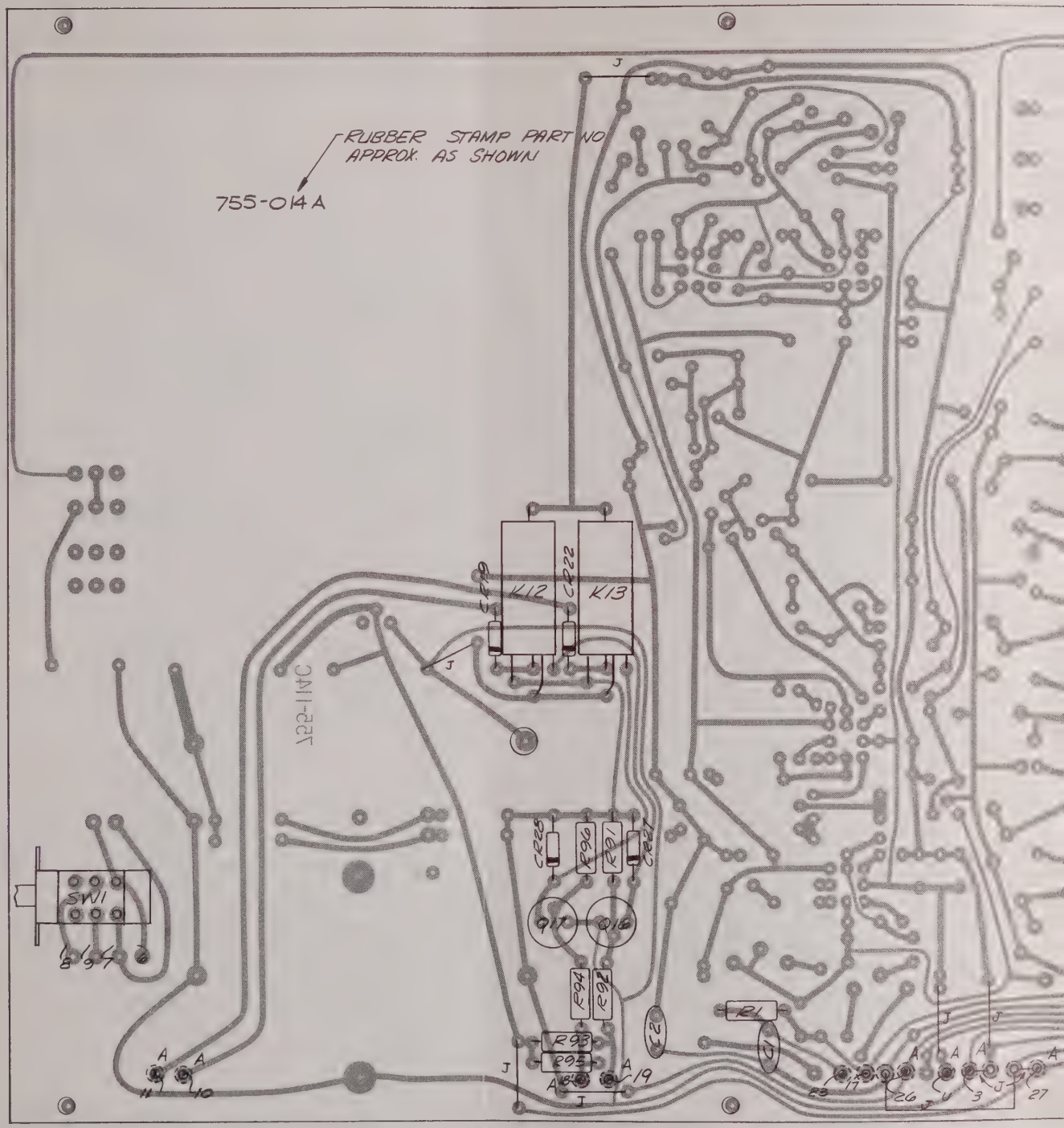
finish N/A

model no. 750/1755 | dwg no. D750-212 | rev D

this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.



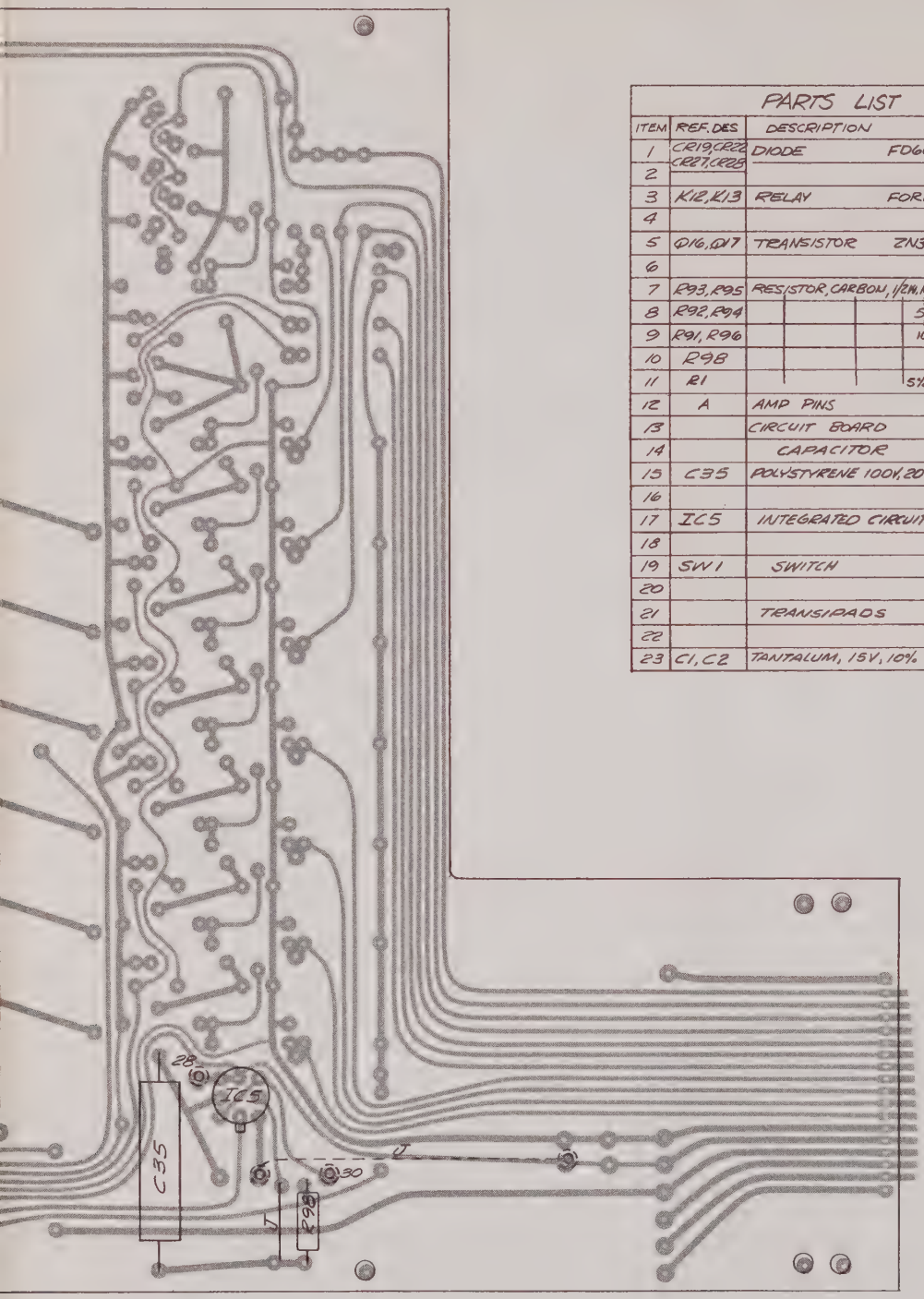




NOTES: UNLESS OTHERWISE SPECIFIED

1 NUMBERED + LETTERED TERMINATIONS ARE FOR WIRING PURPOSES, SEE SCHEMATIC 755-200

2. AMP PINS MOUNTED ON CIRCUIT SIDE

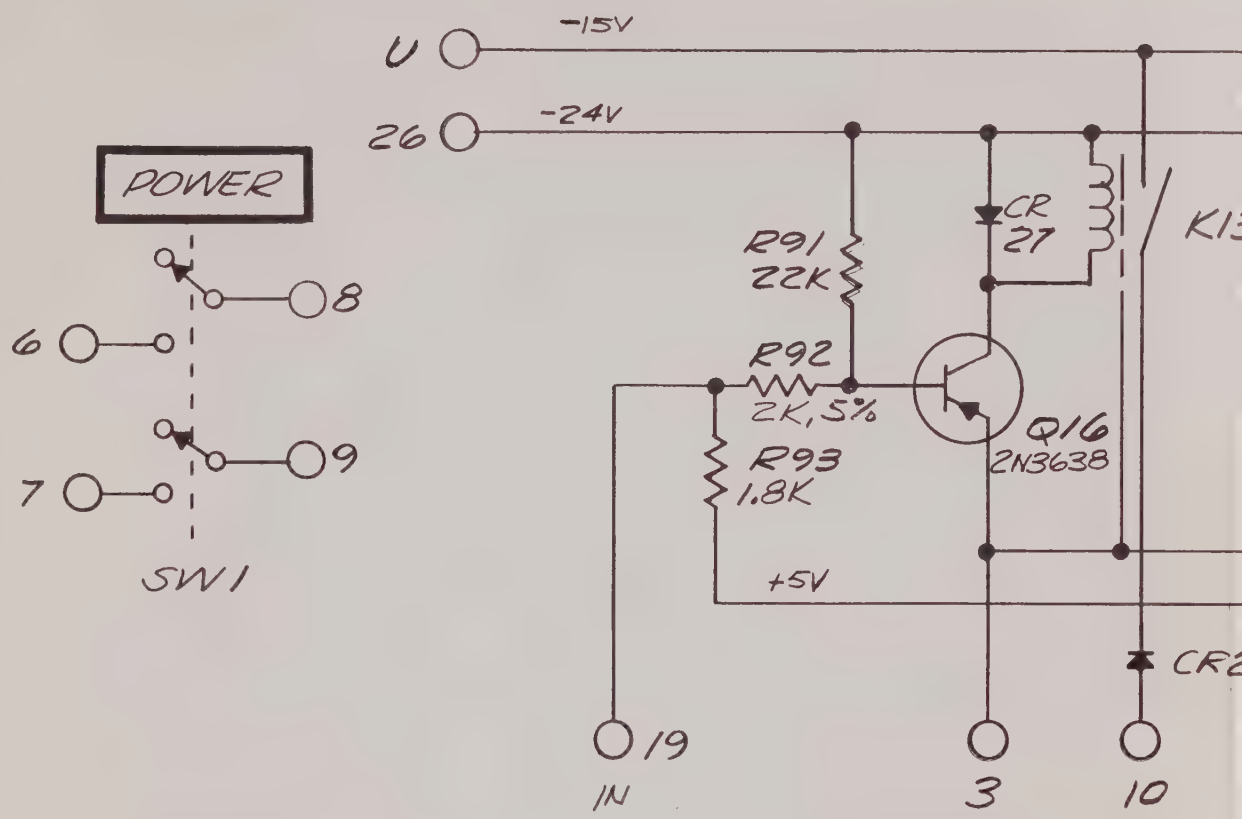


PARTS LIST

ITEM	REF. DES	DESCRIPTION	MFGR	MFGR NO	QTY
1	CR19,CR22 CR27,CR25	DIODE FD6666	FAIRCHILD	FD6666	4
2					
3	K12,K13	RELAY FORM A	JENCO	RR30-1024	2
4					
5	Q16,Q17	TRANSISTOR 2N3638	FAIRCHILD	2N3638	2
6					
7	R93,R95	RESISTOR, CARBON, 1/2W, 10% 1.8K	STACKPOLE	RC20GF 182K	2
8	R92,R94	5% 2K		202J	2
9	R91,R96	10% 22K		223K	2
10	R98	1K		102K	1
11	R1	5% 270Ω		271J	1
12	A	AMP PINS	AMP	61182-2	8
13		CIRCUIT BOARD	WAVETEK	755-114B	1
14		CAPACITOR			
15	C35	POLYSTYRENE 100V, 20%, .1μF	IMB	PA2B104	1
16					
17	IC5	INTEGRATED CIRCUIT	FAIRCHILD	μL914	1
18					
19	SW1	SWITCH	WAVETEK	740-400	1
20					
21		TRANSIPADS	MILTON ROSS	10123N	2
22					
23	C1, C2	TANTALUM, 15V, 10% 22μF	SPRAGUE	1960226X0015P8	2

tolerance unless otherwise specified .XXX ± .010 .XX ± .030	rev	ecn	by	date / app.
	WAVETEK san diego, calif			
scale N/A	by BOCHICHIO	date 7/9/70	app.	
material N/A	title ASSEMBLY, — MIN-MAX CALIBRATION			
finish N/A	model no. 755	dwg no. D755-014	rev	

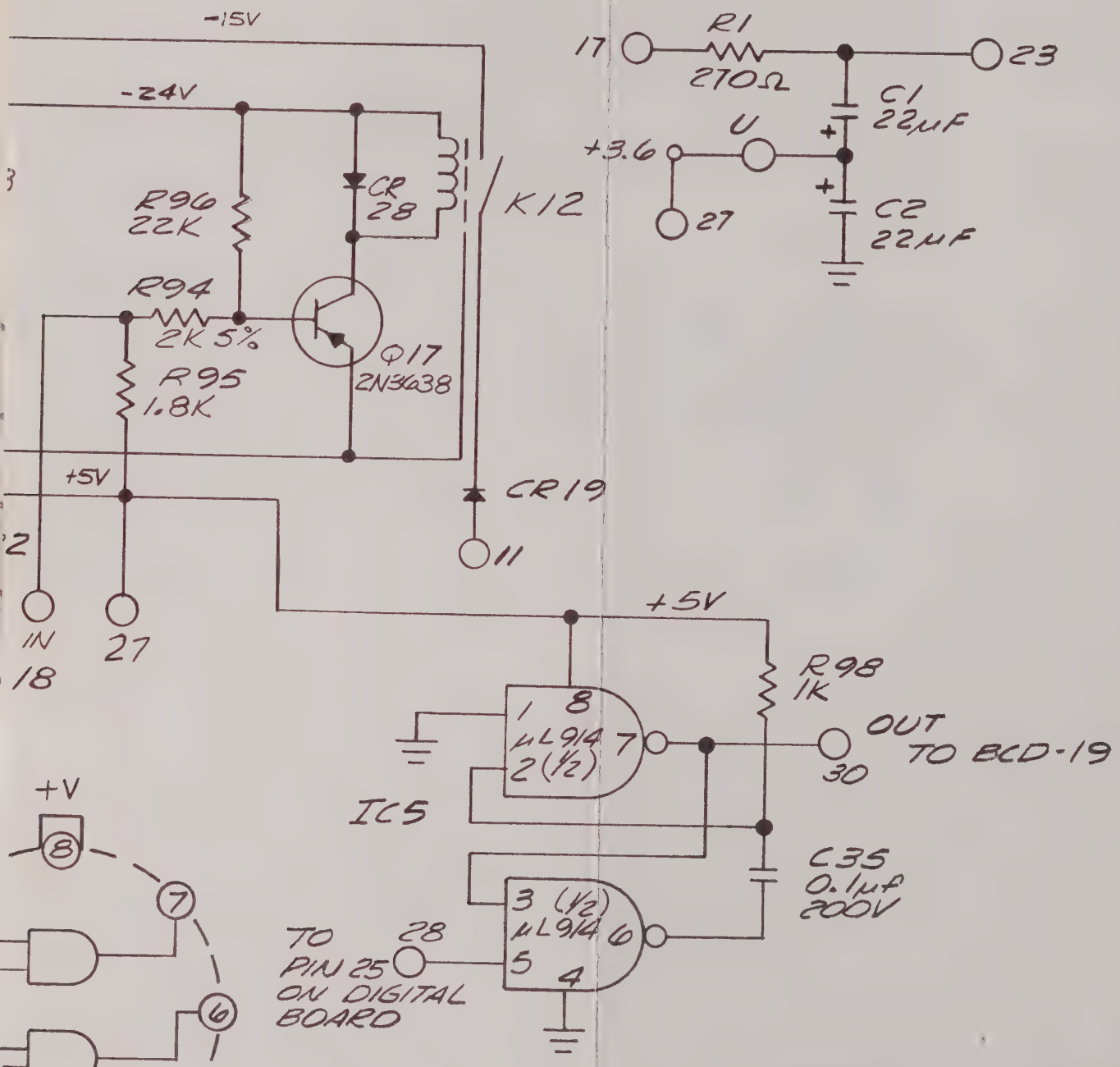
this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.



NOTES: UNLESS OTHERWISE SPECIFIED

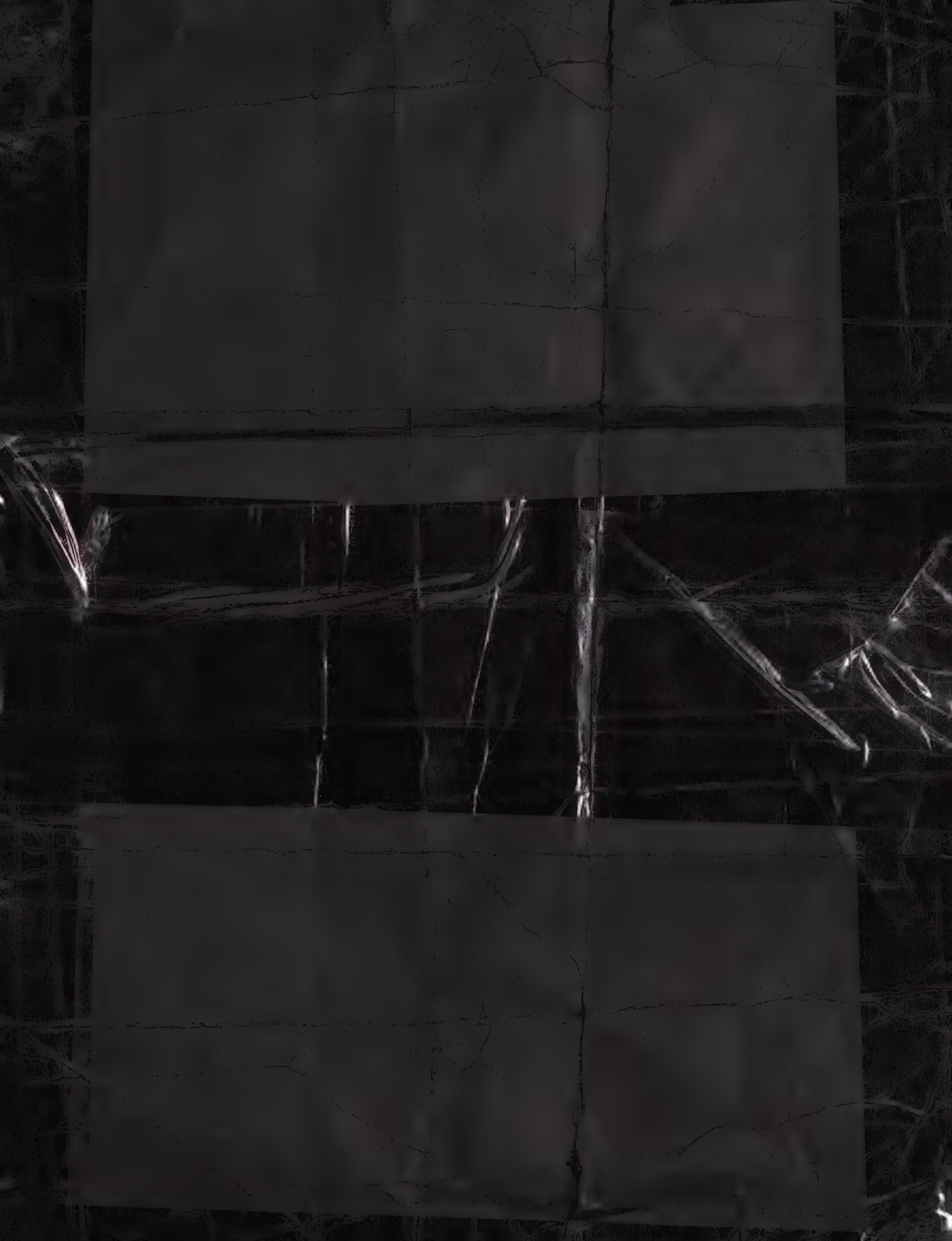
1) RESISTORS ARE 1/2W 10% CARBON
2) DIODES ARE FD6666
3) RELAYS ARE JENCO RR30-1024
4) NUMBERED AND LETTERED TERMINATIONS INDICATE WIRING POINTS. SEE SCHEMATIC 755-200

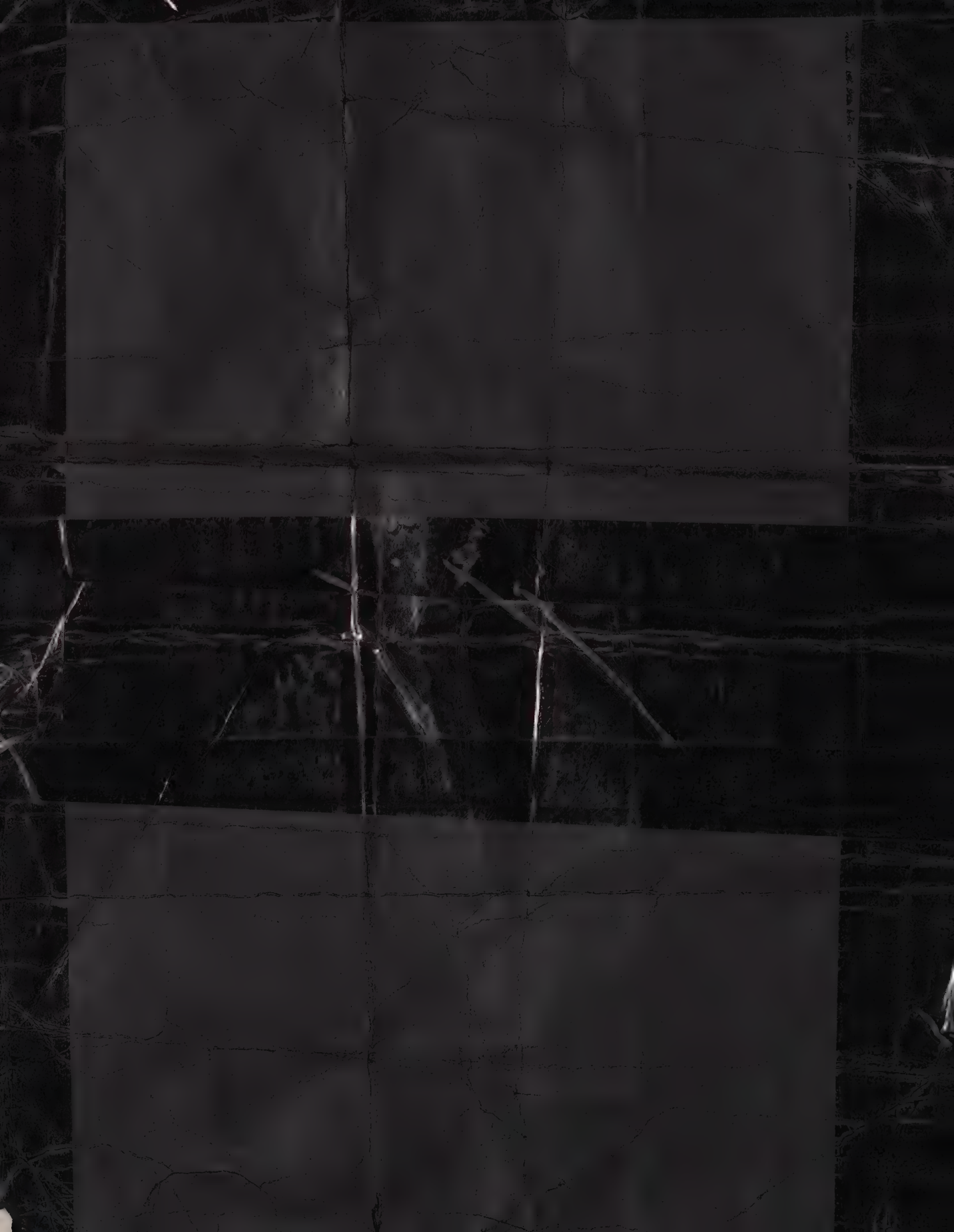
μL914

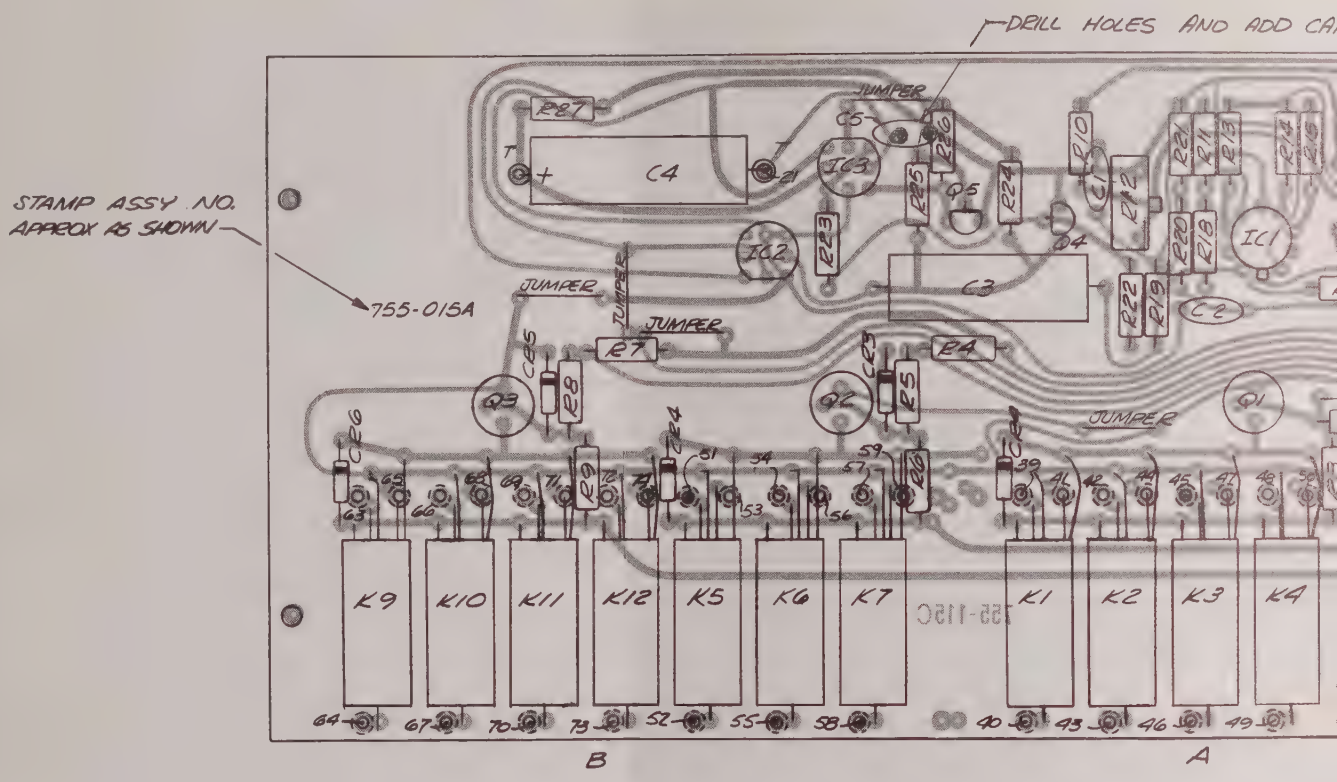


TOLERANCE UNLESS OTHERWISE SPEC	REV	ECN	BY	DATE	APP
.XXX ± .010 .XX ± .030 ANGLES ± 0°30'	WAVETEK SAN DIEGO, CALIF.				
SCALE	BY Bo	DATE 7/9/70	APP		
MATERIAL N/A	TITLE SCHEMATIC MIN-MAX CALIBRATION				
FINISH N/A	MODEL NO. 755	DWG NO B755-214	REV		

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION







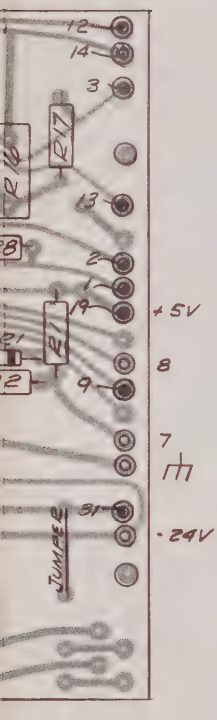
NOTES UNLESS OTHERWISE SPECIFIED

1 ◎ INDICATES AMP PIN INSTALLED ON CIRCUIT SIDE

◎ " " " " COMPONENT SIDE

2 NUMBERED TERMINATIONS INDICATE WIRING POINTS SEE SCHEMATIC 755-200

XCITOR



PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
1		CAPACITOR			
2	C1, C2	CERAMIC DISC, 20V .1μf	CRL	UK20-104	2
3	C3	MYLAR 200V 1μf	ELECTRO CUBE	2108IC-105F	1
4	C4	ELECTROLYTIC 12V, 200 mf	SPRAGUE	TE 1137	1
5	C5	CERAMIC DISC, 1K .001μF	CRL	DD 102	1
6					
7					
8					
9	CR1-CR6	DIODE FD6666	FAIRCHILD	FD6666	6
10					
11					
12		INTEGRATED CIRCUITS			
13	IC1	DUAL COMPARATOR	FAIRCHILD	μA711	1
14	IC3	DUAL INPUT GATE		μL914	1
15	IC2	JK FLIP FLOP		μL923	1
16					
17					
18					
19	K1-K7, K9-K12	RELAY FORM C	JENCO	RR30-1023	11
20					
21	Q1, Q3	TRANSISTOR 2N3638A	FAIRCHILD	2N3638A	2
22	Q2	2N3638	FAIRCHILD	2N3638	1
23	Q4, Q5	2N3646		2N3646	2
24					
25					
26		RESISTOR			
27	R20, R21	CARBON, ½W, 10%, 470Ω	STACKPOLE	RC20GF 471K	2
28	R15, R23	510Ω		511K	2
29	R11, R13, R14, R24, R25, R26	1K		102K	5
30	R1, R4, R7, R28	1.8K		182K	4
31	R2, R5, R8, R24	5% 2K		202J	4
32	R10, R17	10% 5.1K		512K	2
33	R22, R27	10K		103K	2
34	R3, R6, R9	22K		223K	3
35	R18, R19	47K		473K	2
36					
37					
38					
39					
40	R12, R16	POTENTIOMETER 1K	CRL	BA1603-803	2
41					
42	T	TERMINALS	USECO	20108-1	2
43	◎ ◎	AMP PINS	AMP	61182-2	42
44		TRANSIPADS (Q1)	MILTON ROSS	10123N	1
45					
46		CIRCUIT BOARD	WAVETEK	755-115A	1
47					
48					
49					
50					

rev	ecn	by	date	app.
B	ADD AMPL PROG	NG	4-20-70	

tolerance unless otherwise specified
.XXX ± .010
.XX ± .030

WAVETEK san diego, calif

scale N/A | by BOCHICHIO | date 4-18-70 | app

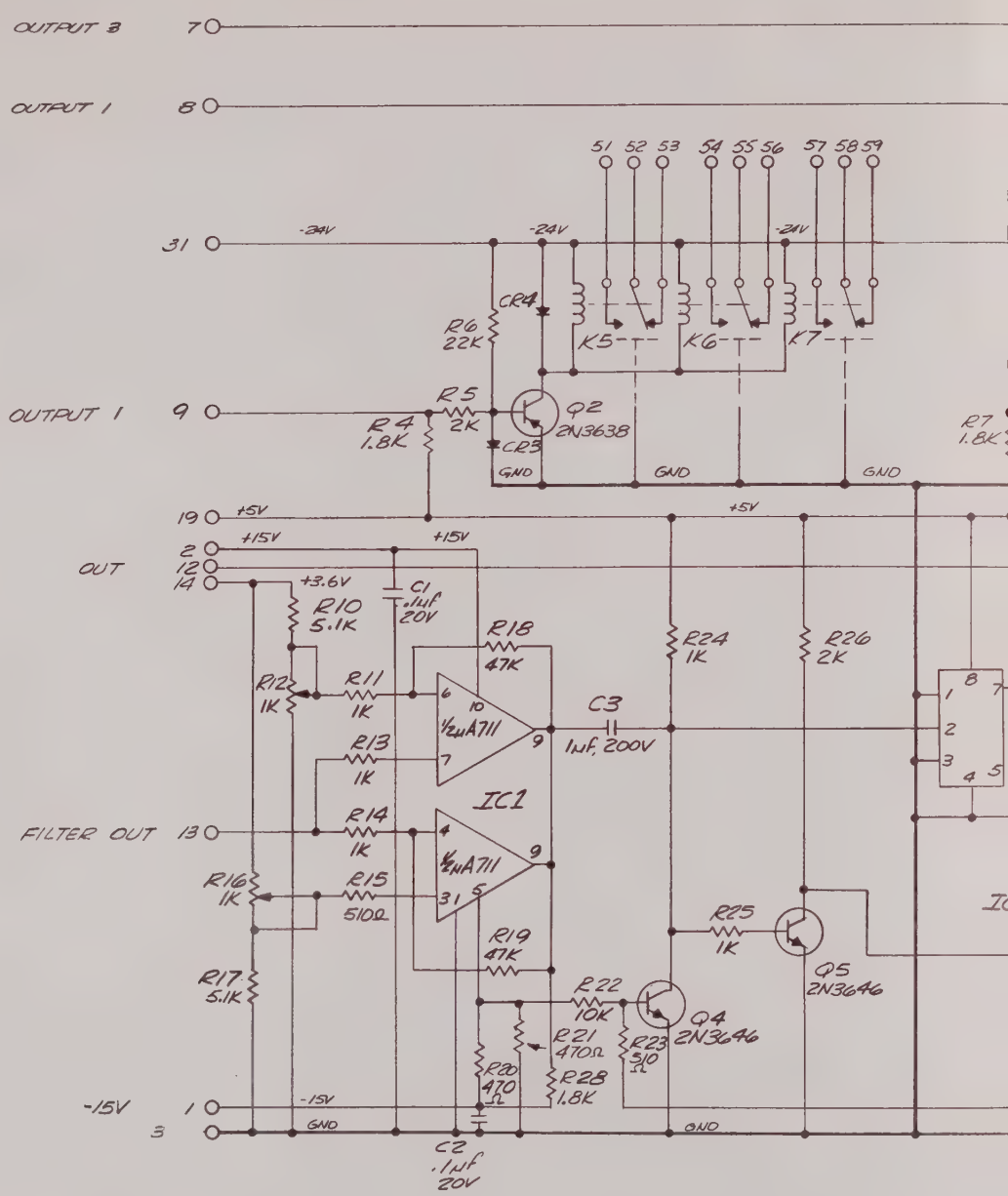
material: N/A

finish: N/A

title: ASSEMBLY AUTO RANGE BD

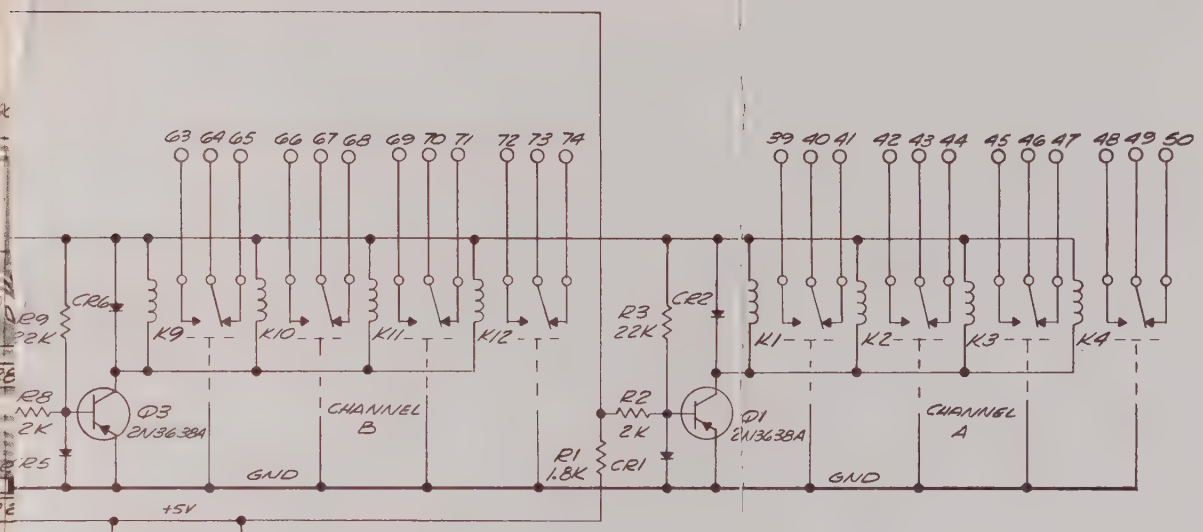
model no. 75B | dwg no. D755-015 | rev B

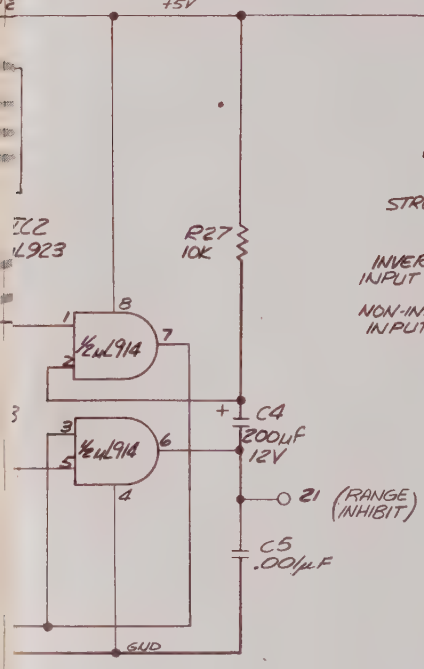
this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.

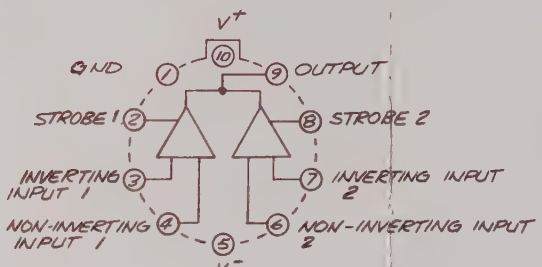


NOTES UNLESS OTHERWISE SPECIFIED

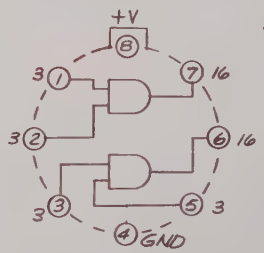
1 RESISTORS ARE CARBON, 10%, 1/2W
2 DIODES ARE FD6666
3 RELAYS ARE JENCO RR30-1023 OR
4 NUMBERED TERMINATIONS INDICATE POINTS. SEE SCHEMATIC 755-20



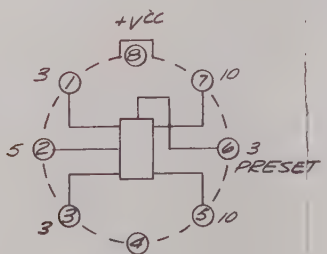




LOGIC DIAGRAM
µL711
(COMPONENT SIDE)



LOGIC DIAGRAM
µL914
(COMPONENT SIDE)

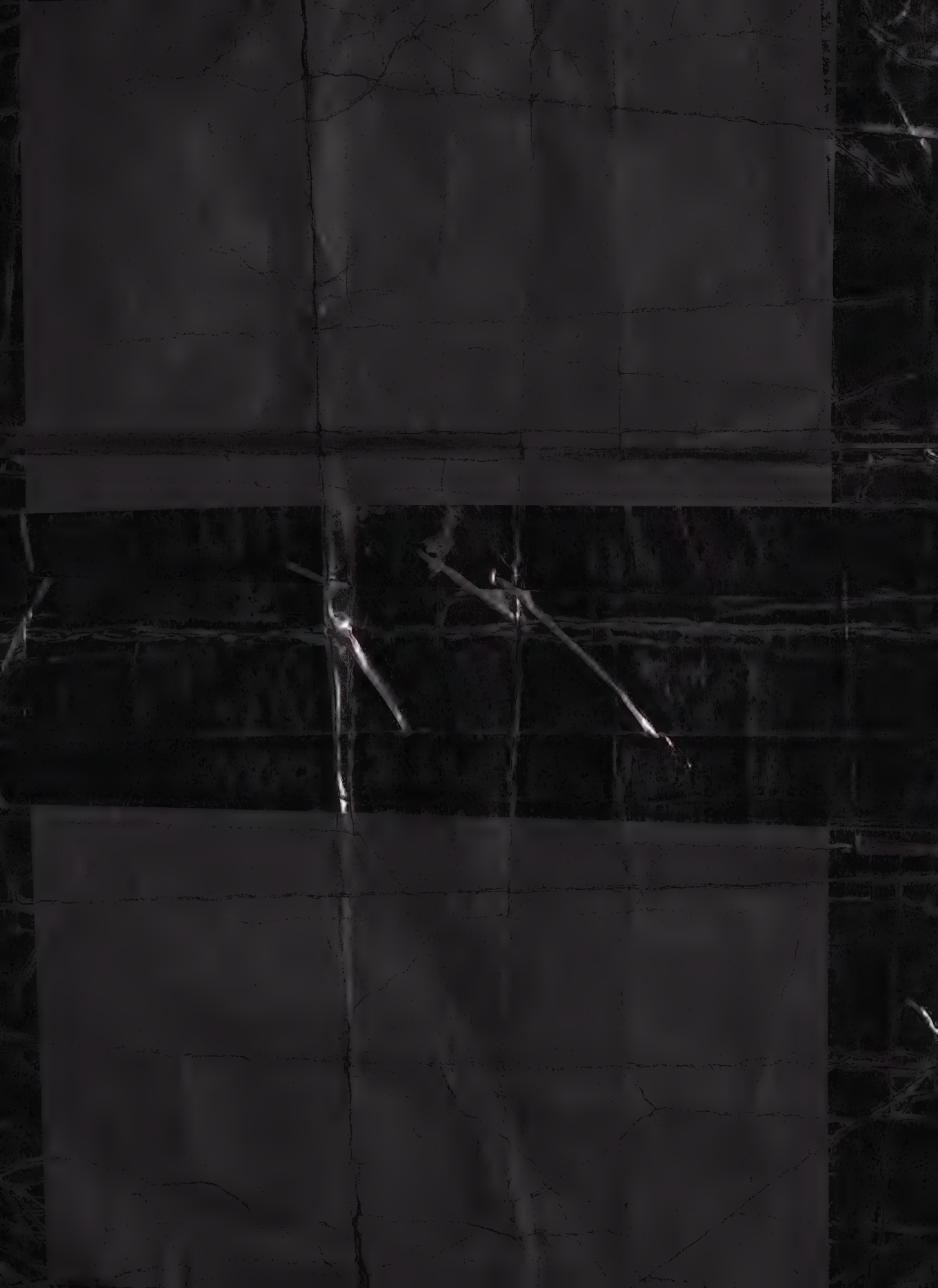


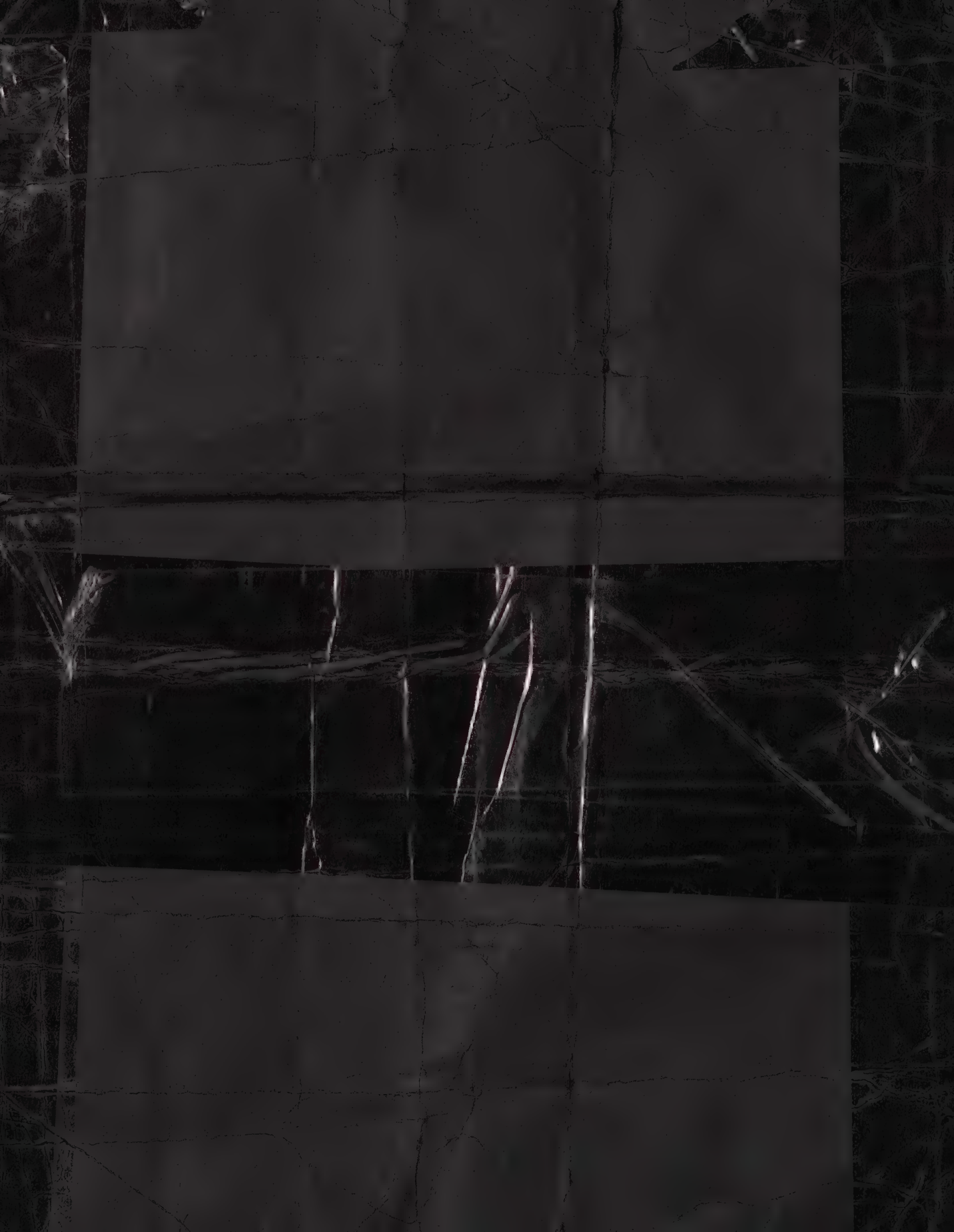
LOGIC DIAGRAM
µL923
(COMPONENT SIDE)

DUIN WIRING

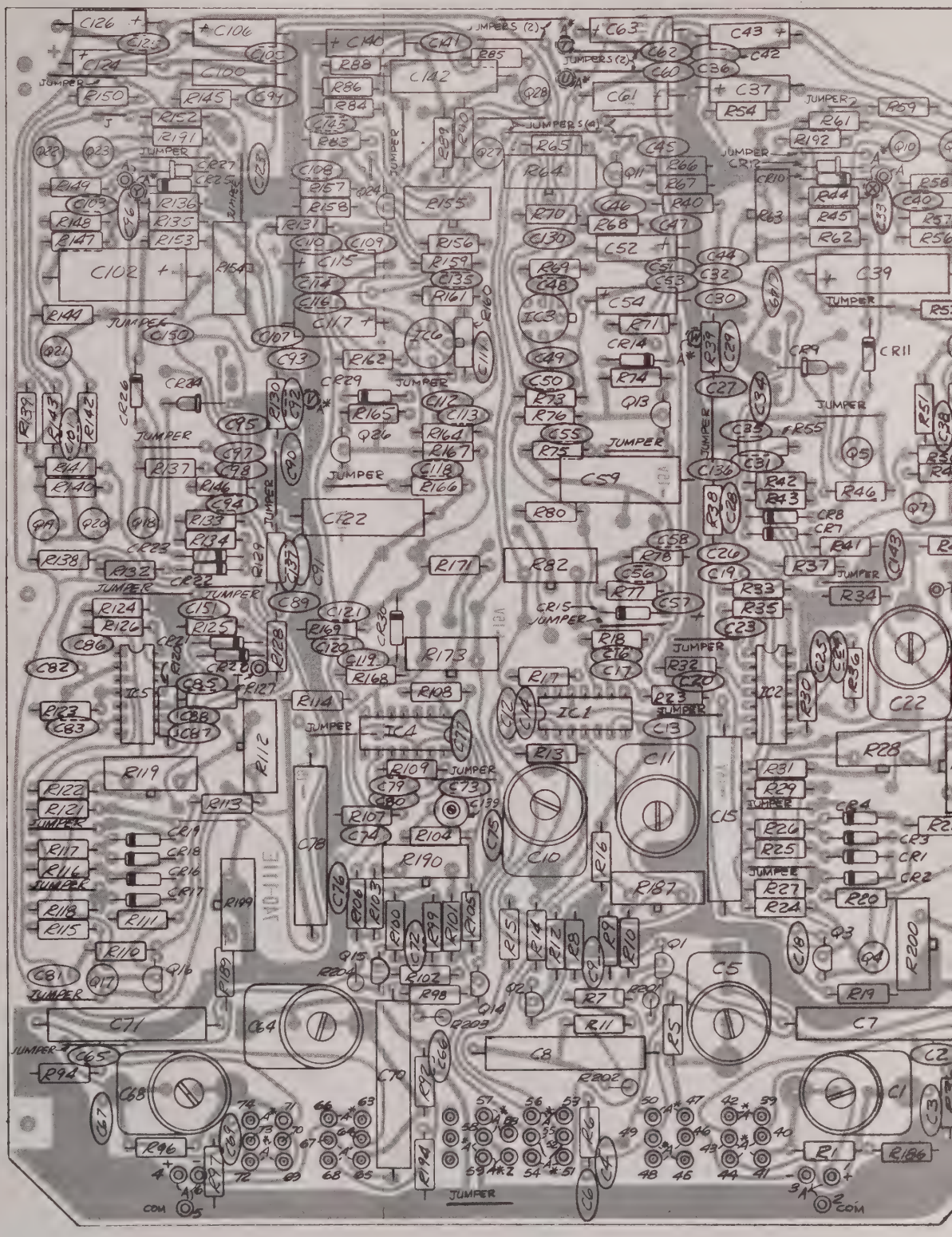
	A	ADD AMPL PROG	NG	4-16-71	
tolerance unless otherwise specified .XXX ± .010 .XX ± .030	rev	ecn	by	date	app.
	WAVETEK san diego, calif.				
scale N/A	by BOCHKHIO	date 4-18-70	app.		
material N/A	title SCHEMATIC AUTO RANGE B'D				
finish N/A	model no. 755	dwg no. D755-215			rev A

this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.





CHANNEL B | CHANNEL A



NOTES: UNLESS OTHERWISE SPECIFIED

1. "A*" INDICATES AMP PIN MOUNTED ON CIRCUIT SIDE; "A", AMP PIN MOUNTED COMPONENT SIDE.
2. FOR INTERCONNECTIONS REFER SCHEMATIC D755-200
3. "J" INDICATES JUMPER.
4. LETTER DESIGNATIONS ARE INTERCONNECTION POINTS.

PARTS LIST

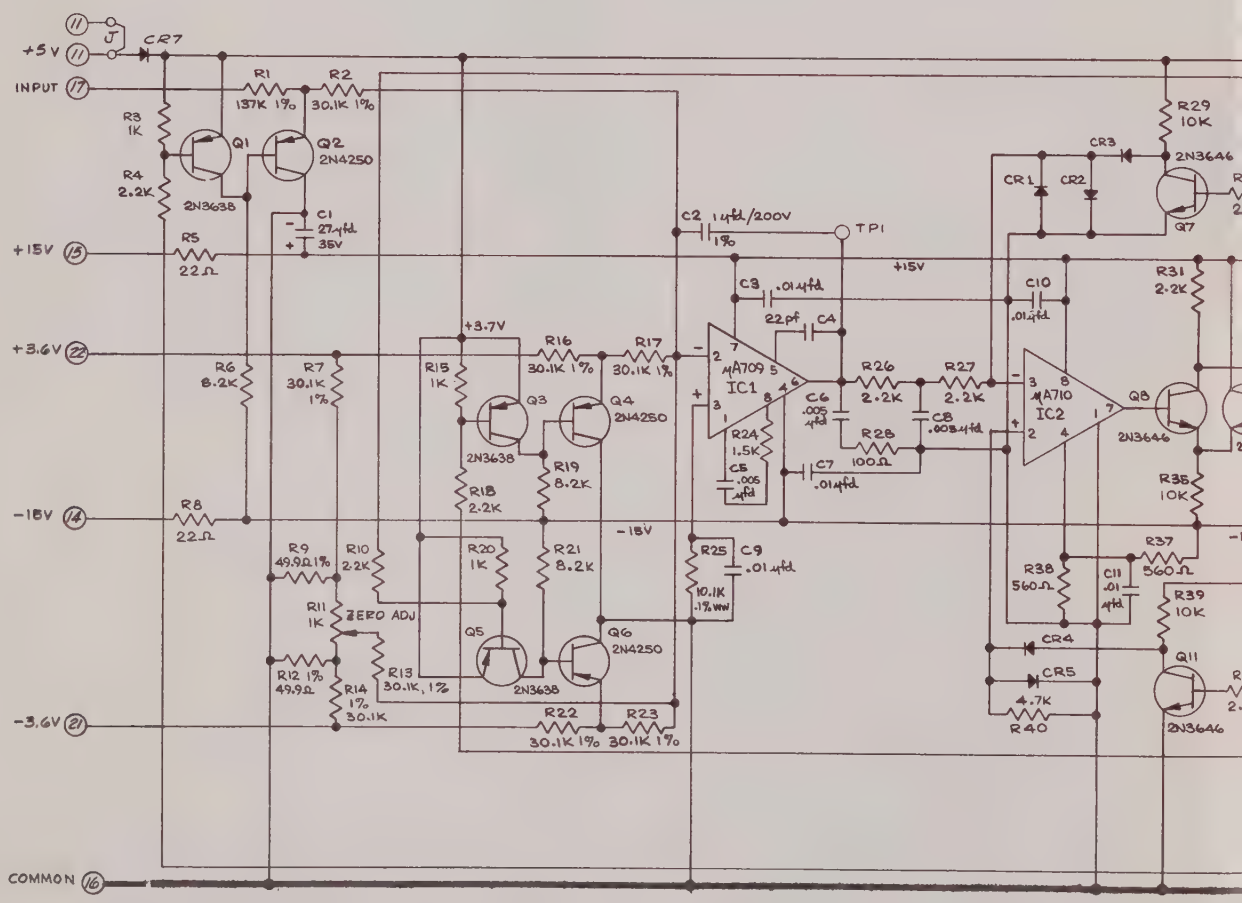
ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
1	C2, C6, C65 C69, C73 C81, C86	CERAMIC DISC 1000V 5pF	CRL	DD-050	6
2	C130, C135	1.5 pF	SPRAGUE	10TCC-V15	2
3	C28, C29, C34, C86-C88	10pF	CRL	DD-100	7
4	C18, C81	15pF		DD-150	2
5	C14, C17, C49 C77, C80, C148, C112 C149, C150, C151	22pF		DD-220	10
6	C16, C38 (alt) C79, C101, C10	100pF		DD-101	6
7	C48, C111	220pF		DD-221	2
8	C33, C34, C96, C97	330pF		DD-331	4
9	C4, C56 C103, C119	470pF		DD-471	4
10	C55, C118	1500pF		DD-152	2
11	C23, C30, C91, C93	.05µF		CK-503	4
12	C9, C35, C36 C42, C51, C53, C60, C62, C72, C98, C99, C105, C114, C116, C125, C141, C142, C143 (alt)	50V .01µF		CK-103	19
13	C8, C13, C18 C20, C31 C40, C45, C50, C58, C75 C76, C82, C83, C94, C102, C113, C121	20V .1µF		UK20-104	18
14	C37, C43, C52 C54, C64, C103 C106, C108 C115, C119 C124, C126, C140	ELECTROLYTIC 15V 5µF	SPRAGUE	5000506806BA7	13
15	C57, C120	TANTALUM .33µF		196D334X0015HB	2
16	C39, C102	ELECTROLYTIC 16V 100µF		5000107016DX7	2
17	C59, C122, C142	MYLAR 100V, 10% .1µF	CDE	WMF-1P1E	3
18	C7, C8, C75, C10, C11, C78	200V 1% 1µF	ELECTRO CUBE	2108IC-105F	6
19	C1, C5, C10, C11 C22, C44, C48	VARIABLE CAPACITOR 4.5-25pF	ERIE	503-001-37A	7
20	C136, C137	SELECTED VALUE			2
21	C139	VARIABLE CAPACITOR 3.5-13pF	STETTNER	75-TRIKO-02	1
22	C3, C66, C67	S.M. (-36) 910pF	ARCO	DM15-911F	4
23	C24, C25, C26, C27, C28	CERAMIC DISC 50V .1µF	CRL	CK104	6
24	C46, C109	MYLAR 50V .1µF	GB	GSF13AA104	2
25					
26	CR1-CR4, CR7, CR8, CR15, CR16, CR19, CR22, CR23, CR25, CR29, CR30	DIODE	FAIRCHILD	FD6666	18
27	CR11, CR26			IN34A	2
28	CR18, CR27		G.E.	IN3716	2
29	CR9, CR24			IN3717	2
30	CR5+6 CR20+21	(-42)	H.P.	HP2811	4
31					
32					
33					
34					
35	IC3, IC6	INTEGRATED CIRCUIT	FAIRCHILD	µA709	2
36	IC1, 2, 4, 5	(-40)	RCA	CA3030	4
37					
38					
39					
40					
41					
42	Q5, Q19, Q20, Q23	TRANSISTORS	FAIRCHILD	2N3640	4
43	Q4, Q6-Q9 Q17, Q18 - Q22, Q27			2N3646	11
44	Q28		MOTOROLA	2N4851	1
45	Q11, Q13, Q24, Q26			MPF-104	4
46	Q1, Q2 Q14, Q15	(-37)		MPF-104	4
47	Q3, Q16	(-38)		MPF-104	2
48					
49					
50					
51	R63, R154	POTENTIOMETER 500Ω	CRL	BA1603-B02	2
52	R21, R200 R112, R149 R190, R187	10K		-B05	6
53	R28, R82 R119, R173	100K		-B19	4
54	R64, R155	10K	A/B	FR103M	2
55					

PARTS LIST

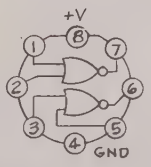
ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO	QTY
56	R66, R157	METAL FILM 1/4W 1% 46.4Ω	CORNING	RN60D	2
57	R62, R65 R153, R156	1% 3.32K			4
58	R42, R43 R133, R134	4.99K			4
59	R14, R15, R106, R106	10K(-4)			4
60	R86	12.1K			1
61	R13, R16, R104, R107	12.1K(-33)			4
62	R40, R131	27.4K			2
63	R7, R11, R98, R102	1MΩ			4
64	R1, R5, R92, R96	1MΩ(-34)			4
65	R186, R194	47.5K			2
66	R193, R189	46.4K			2
67					
68					
69					
70	R48, R54, R71, R73, R89, R139 R145, R162, R164,	CARBON 1/2W 5% 47Ω	STACKPOLE	RC20GF470J	9
71	R89	68Ω		680J	1
72	R3, R6, R19 R32, R58, R94 R97, R110, R123 R149	10% 100Ω		101K	10
73	R41, R138 R29, R121	150Ω		151K	4
74	R47, R55, R57, R134 R146, R144	470Ω		471K	6
75	R45, R61, R67 R68, R70, R89, R136, R152, R156, R159, R169	1K		102K	11
76	R17, R18, R35 R84, R93, R129, R85, R105 R109, R120, R127 R150, R160	1.5K		152K	13
77	R53, R90, R142, R201-R204	2.2K		222K	7
78	R8, R99	2.7K		272K	2
79	R191, R192	3.3K		332K	2
80	R34, R125	3.9K		392K	2
81	R22, R30, R44 R49, R52, R113, R135, R140, R143 R120,	4.7K		472K	10
82	R25, R116	5.6K		562K	2
83	R10, R12, R101, R103	6.8K		682K	4
84	R9, R100	5% 7.5K		752J	2
85	R84	10% 9.1K		912K	1
86	R20, R26, R27, R51, R52, R77, R80, R111 R117, R118 R142, R147, R163, R171	10K		103K	14
87	R24, R115	22K		223K	2
88	R46, R137	27K		273K	2
89	R31, R39, R75 R124, R184, R146	47K		473K	6
90	R50, R141	62K		623K	2
91	R76, R167	150K		154K	2
92	R74, R165	270K		274K	2
93	R23, R114	470K		474K	2
94	R37-R39 R128-R130	1MΩ		105K	6
95	R70, R161	2.2MΩ		225K	2
96					
97					
98		CIRCUIT BOARD	WAVETEK	740-111E	1
99					
100	◎ T	TERMINALS	USECO	2010B-1	2
101					
102	○ A	AMP PINS	AMP	61182-2	16
103					
104					
105					

tolerance unless otherwise specified	rev	ecn	by	date	app.
.XXX ± .010 .XX ± .030	WAVETEK san diego, calif				
scale N/A	by GRAY	date 10/12/70	app		
material N/A	title ASSY ZERO CROSSING BD				
finish N/A	model no. 755	dwg no. D755-011	rev		

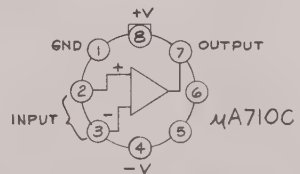
this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.



CμL914



μA710C



LAST COMP DES USED

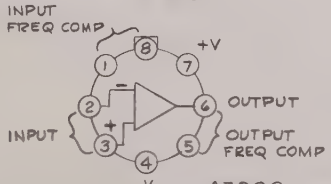
R54 TP6
C18 Q17
CR7 IC7

NOTES:- UNLESS OTHERWISE SPECIFIED-

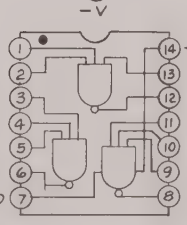
1. ALL DIODES FD6666
2. ALL RESISTORS ½ WATT, 10%, CARBON
3.
4.
5.
6. IC3 & IC4 ARE MC863P
7. IC5 IS MC856P
8. IC6 & IC7 ARE CμL914
9. FOR INTERCONNECTION SEE D750-200

10* R53 & R55, 12.1K MF ON STANDARD 755

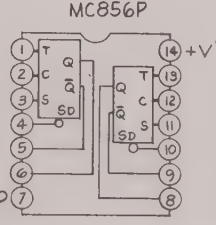
μA709C

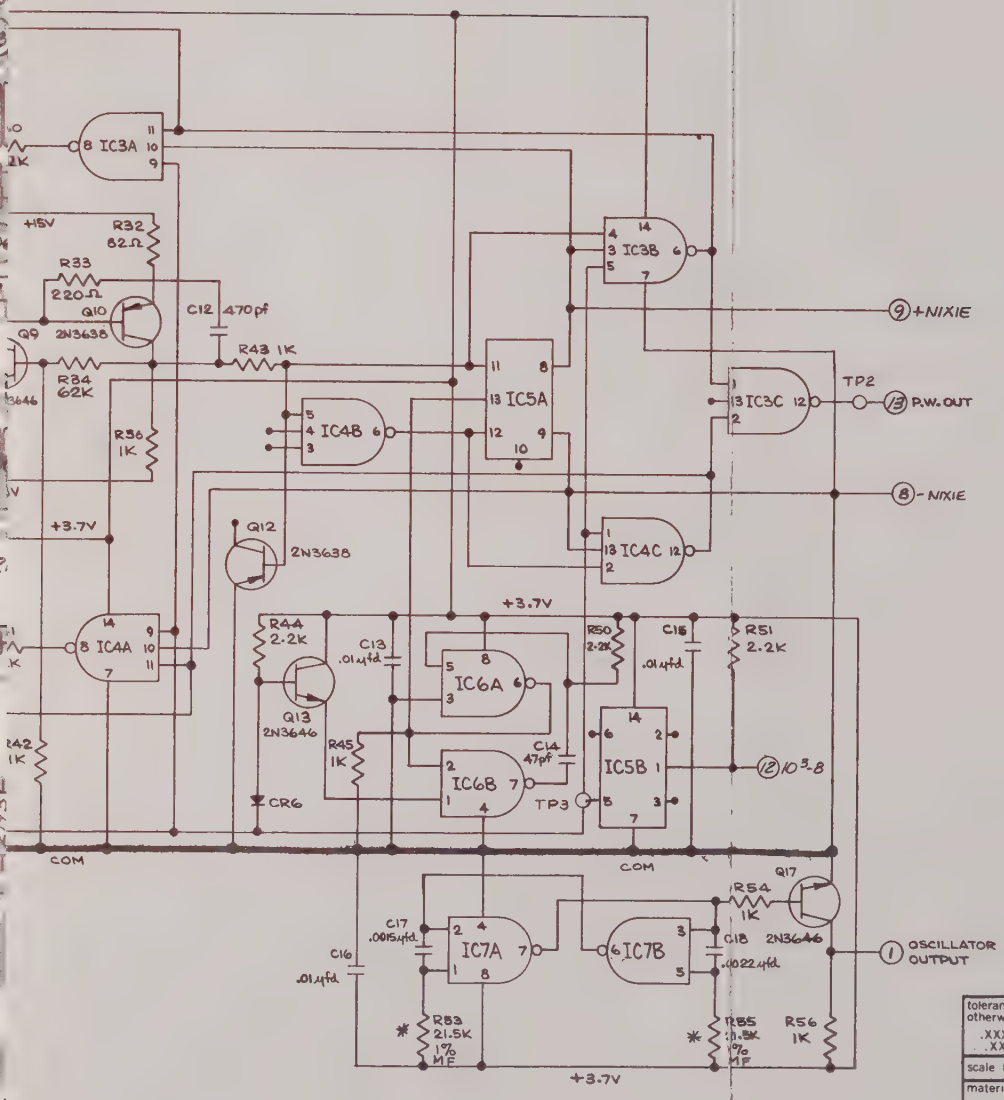


MC863P



MC856P





rev	ecn	by	date	app.
B	ECN 317	NG	7/6/70	
A	ECN 306	NG	7/15/70	

tolerance unless otherwise specified
.XXX ± .010
..XX ± .030

WAVETEK san diego, calif.

scale N/A | by MAST | date 25 NOV 69 | app.

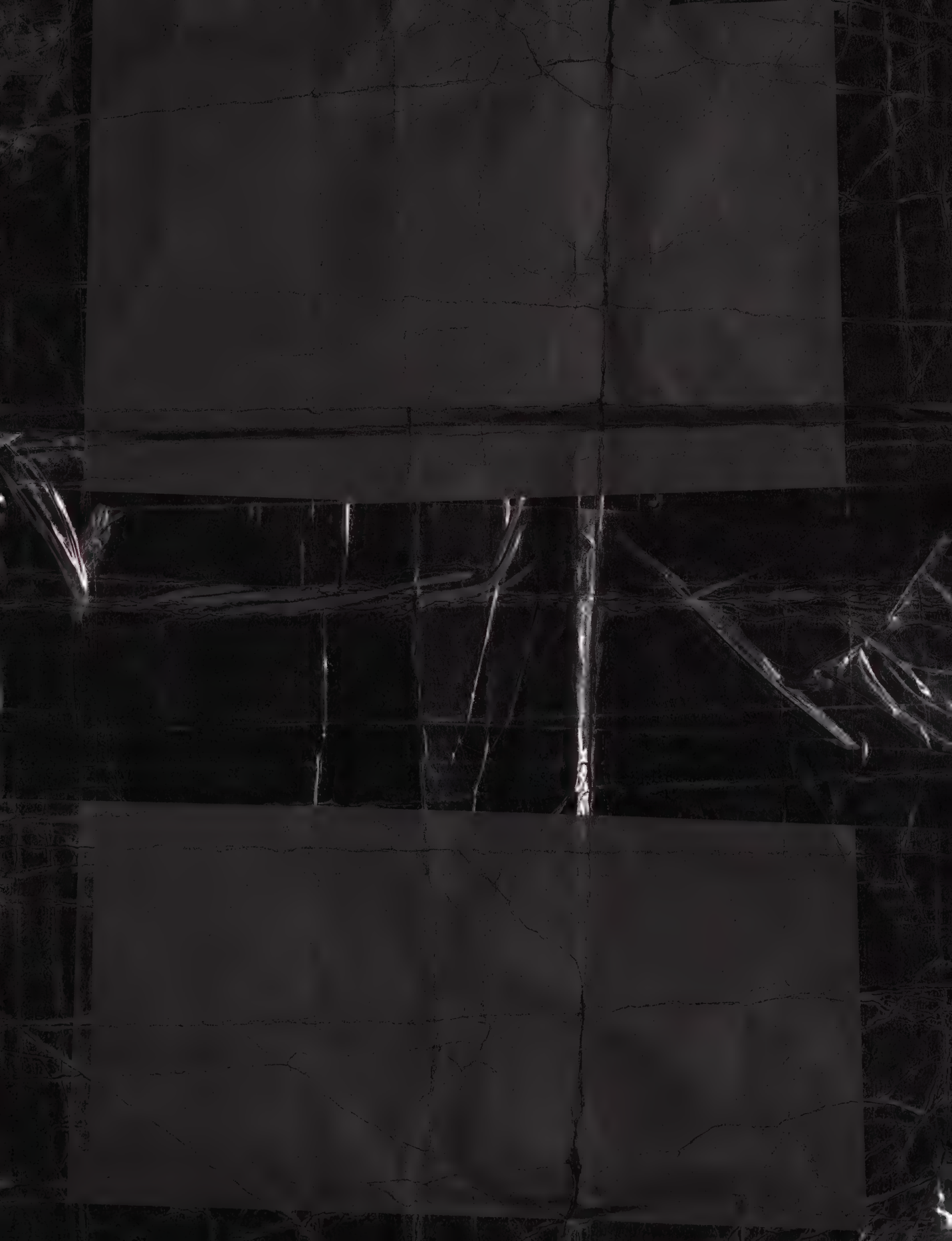
material N/A

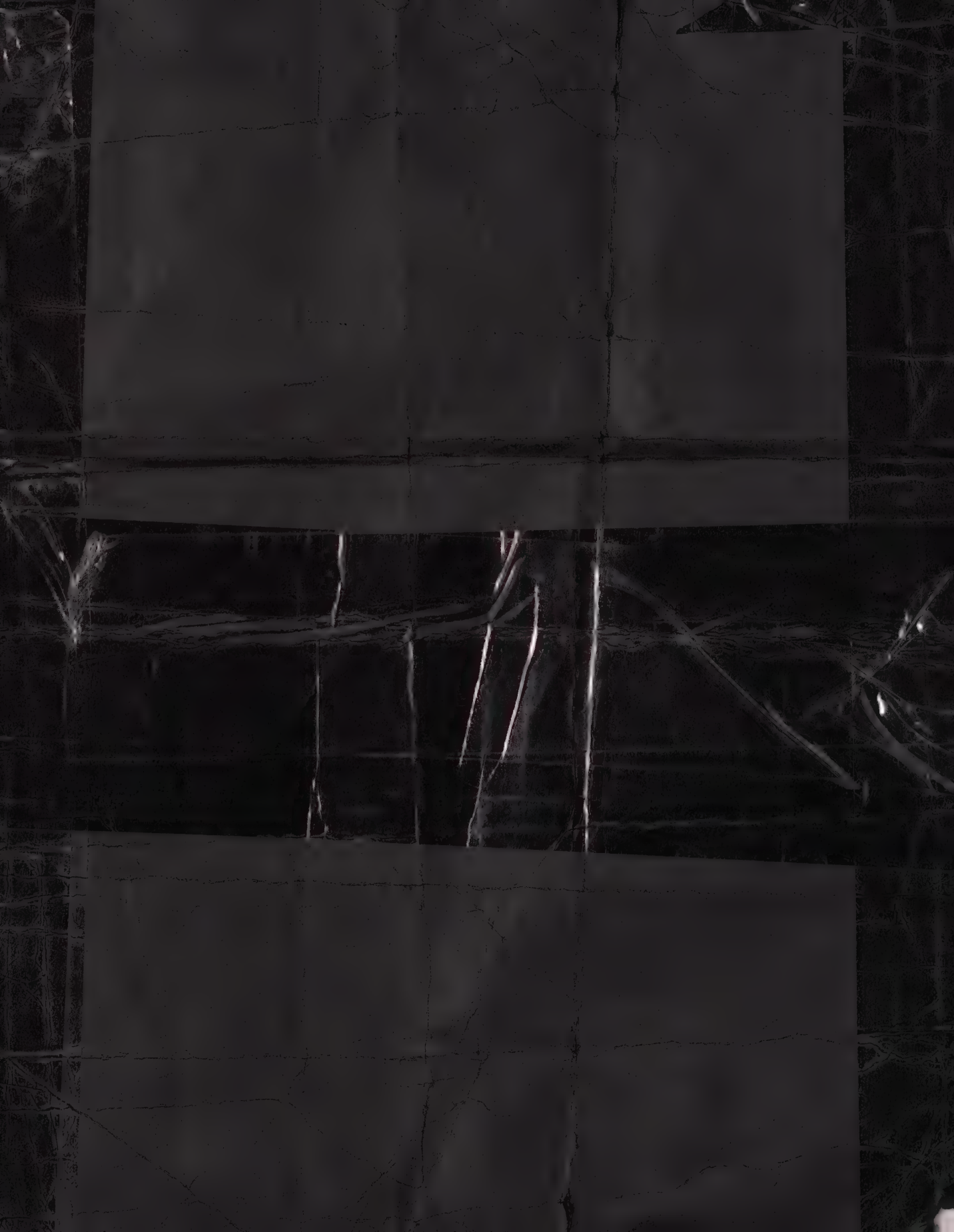
finish N/A

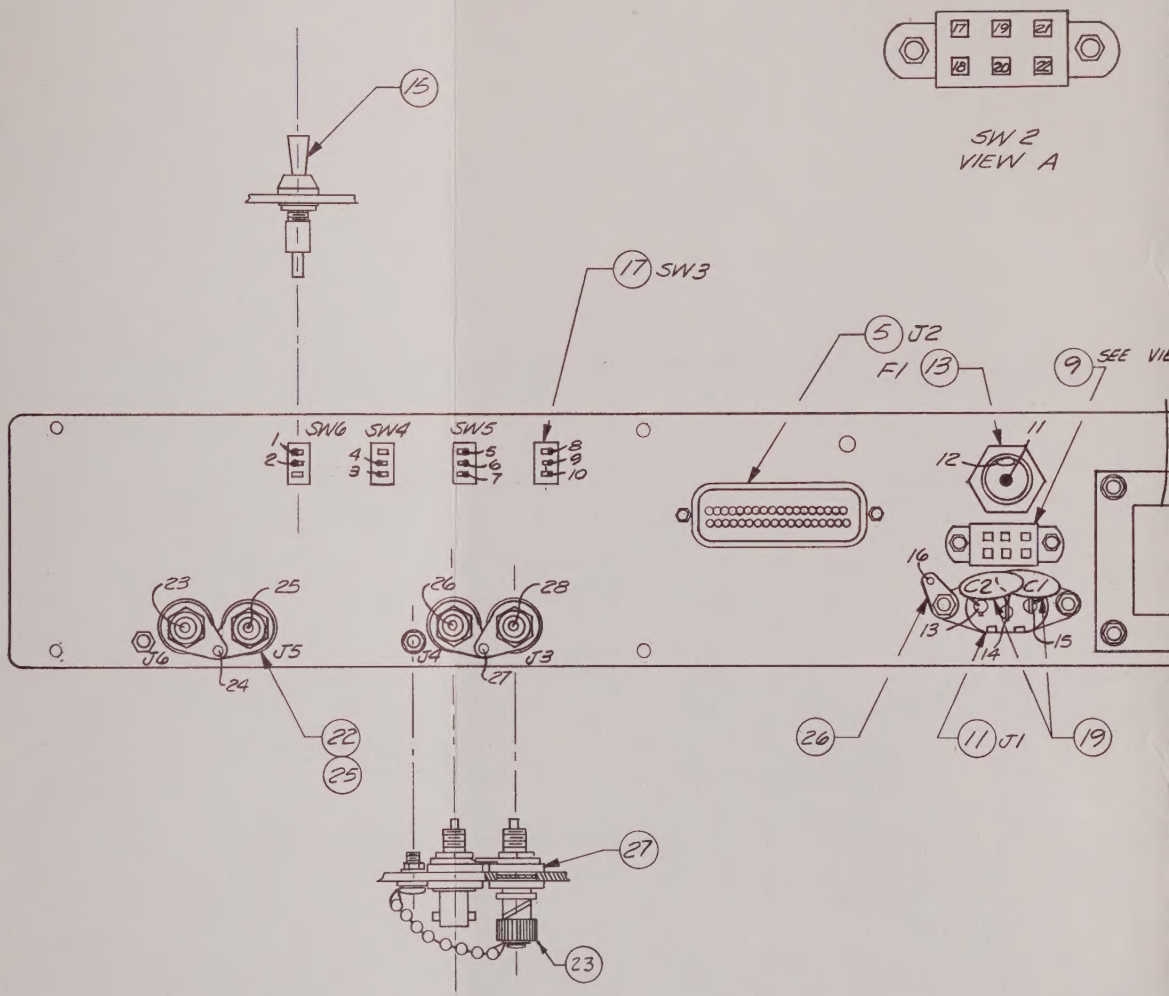
title: SCHEMATIC, ANALOG BOARD

model no. 270,750, 755 | dwg no. D270-211 | rev B

this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.







NOTES: UNLESS OTHERWISE SPECIFIED

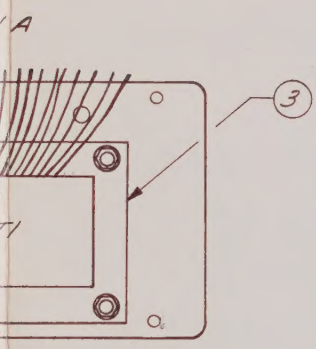
1. NUMBERED TERMINATIONS INDICATE WIRING POINTS, SEE SCHEMATIC 755-200

T1
TRANSFORMER WIRING LIST

COLOR	DESTINATION	PIN NO
RED	LOGIC + POWER SUPPLY	BU
RED		BT
GREEN		BS
GREEN		BR
BLUE		BQ
BLUE/WHT		BP
BLUE		BN
GRAY	REAR PANEL	19
GRY/WHT		18
BLACK		17
BLK/WHT		20

PARTS LIST

ITEM	REF DES	DESCRIPTION	MFGR	MFGR NO.	QTY
1		REAR PANEL	WAVETEK	755-315	1
2					
3	T1	TRANSFORMER	WAVETEK	750-500	1
4					
5	J2	CONNECTOR SOCKET	AMPHENOL	57-40360	1
6		" PLUG	"	57-30360	1
7					
8					
9	SW2	LINE SWITCH (115-230V)	SWITCH CRAFT	46256LF	1
10					
11	J1	POWER RECEPTACLE	SWITCH CRAFT	AC3G	1
12	F1	FUSE HOLDER	LITTELFUSE	342-012	1
13		FUSE 230V, 1/4 AMP SB		313-250	1
14		FUSE 115V, 1/2 AMP SB		313-.500	1
15	SW4, SW5 SW6	SWITCH SPOT	C+K	7101-P-DPZ	3
16					
17	SW3	SWITCH, MOMENTARY	C+K	7105-P-DPZ	1
18					
19	C1, C2	CERAMIC DISC, 1KV, .005μF	CRL	DD502	2
20					
21					
22	J3-J6	BNC CONNECTOR	KINGS	KG79-46	4
23		SHORTING CAP	AMPHENOL	31017	2
24					
25		SOLDER LUG	H.H. SMITH	1497	4
26		SOLDER LUG		1414-4	1
27		SHOULDER WASHER		2668	8
28					
29					
30					
31					



J2
PIN CONNECTOR
WIRING LIST

PIN NO.	DESTINATION
1	TO DIGITAL BD 7
2	9
3	10
4	8
5	11
6	13
7	14
8	12
9	15
10	17
11	18
12	16
13	19
14	20
15	C
16	G
17	LOGIC & POWER SUPPLY BE
18	9
19	DIGITAL BD 1
20	LOGIC & POWER SUPPLY 25
21	MIN-MAX CAL 11
22	10
23	NOT USED
24	
25	
26	
27	
28	
29	
30	
31	
32	
33	
34	
35	
36	

tolerance unless otherwise specified .XXX ± .010 .XX ± .030	rev	ecn	by	date	app.
	WAVETEK san diego, calif				
scale FULL	by GRAY	date 7/1/70	app.		
material N/A	title ASSY, REAR PANEL			SHT 2 OF 2	
finish N/A	model no. 755	dwg no. D755-000		rev	

this document contains proprietary information and design rights belonging to WAVETEK and may not be used or reproduced for any reason except calibration, operation and maintenance without written authorization.

MP MASTER
MA35687